

Andries J Scholten

List of Publications by Year in descending order

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42
papers

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44
all docs

44
docs citations

44
times ranked

390
citing authors

#	ARTICLE	IF	CITATIONS
1	Best Practices for Compact Modeling in Verilog-A. IEEE Journal of the Electron Devices Society, 2015, 3, 383-396.	2.1	68
2	RF-Noise Modeling in Advanced CMOS Technologies. IEEE Transactions on Electron Devices, 2014, 61, 245-254.	3.0	40
3	Benchmark Tests for MOSFET Compact Models With Application to the PSP Model. IEEE Transactions on Electron Devices, 2009, 56, 243-251.	3.0	35
4	The Relation Between Degradation Under DC and RF Stress Conditions. IEEE Transactions on Electron Devices, 2011, 58, 2721-2728.	3.0	32
5	A Physics-Based Statistical RTN Model for the Low Frequency Noise in MOSFETs. IEEE Transactions on Electron Devices, 2016, 63, 3683-3692.	3.0	29
6	The New CMC Standard Compact MOS Model PSP: Advantages for RF Applications. IEEE Journal of Solid-State Circuits, 2009, 44, 1415-1424.	5.4	23
7	PSP-SOI: An advanced surface potential based compact model of partially depleted SOI MOSFETs for circuit simulations. Solid-State Electronics, 2009, 53, 18-29.	1.4	20
8	SPECTROSCOPIC STUDY OF CHLOROPHYLL a IN ORGANIC SOLVENTS AND POLYMERIZED ANHYDROUS POLYVINYL MATRIX. Photochemistry and Photobiology, 1993, 58, 600-606.	2.5	19
9	Impact of interface states on MOS transistor mismatch. , 2009, , .		17
10	A physics-based RTN variability model for MOSFETs. , 2014, , .		16
11	Surface-Potential-Based Compact Model of Bulk MOSFET. , 2010, , 3-40.		16
12	Benchmarking the PSP Compact Model for MOS Transistors. , 2007, , .		15
13	Surface-potential-based MOSFET models with introduction to PSP (invited). , 2009, , .		14
14	A Compact Model for Valence-Band Electron Tunneling Current in Partially Depleted SOI MOSFETs. IEEE Transactions on Electron Devices, 2007, 54, 316-322.	3.0	13
15	ESD protection for a 5.5 GHz LNA in 90 nm RF CMOS — Implementation concepts, constraints and solutions. , 2004, , .		12
16	Experimental Demonstration and Modeling of Excess RF Noise in Sub-100-nm CMOS Technologies. IEEE Electron Device Letters, 2010, 31, 884-886.	3.9	11
17	Compact Modeling of Junction Current in Dynamically Depleted SOI MOSFETs. IEEE Transactions on Electron Devices, 2008, 55, 3295-3298.	3.0	10
18	A PSP-Based Small-Signal MOSFET Model for Both Quasi-Static and Nonquasi-Static Operations. IEEE Transactions on Electron Devices, 2008, 55, 1424-1432.	3.0	10

#	ARTICLE	IF	CITATIONS
19	Threshold behavior of the drift region: The missing piece in LDMOS modeling. , 2013, , .		9
20	PSPHV: A Surface-Potential-Based Model for LDMOS Transistors. IEEE Transactions on Electron Devices, 2019, 66, 5246-5253.	3.0	8
21	Autocorrelation Analysis as a Technique to Study Physical Mechanisms of MOSFET Low-Frequency Noise. IEEE Transactions on Electron Devices, 2017, 64, 2919-2926.	3.0	8
22	Comparison of electrical techniques for temperature evaluation in power MOS transistors. , 2013, , .		6
23	A Compact Model for the Statistics of the Low-Frequency Noise of MOSFETs With Laterally Uniform Doping. IEEE Transactions on Electron Devices, 2017, 64, 3331-3336.	3.0	6
24	Benchmark Tests for MOSFET Compact Models. , 2010, , 75-104.		6
25	The JUNCAP2 Model for Junction Diodes. , 2010, , 299-326.		5
26	Modeling and characterization of noise in 90-nm RF CMOS technology. AIP Conference Proceedings, 2005, , .	0.4	4
27	Temperature and geometry dependence of the electrothermal instability of bipolar transistors. , 2012, , .		4
28	Reliability Simulation Models for Hot Carrier Degradation. , 2015, , 477-517.		4
29	New physical insight for analog application in PSP bulk compact model. , 2018, , .		4
30	SiGe HBT PA Design for 5G (28 GHz and Beyond) - Modeling and Design Challenges. , 2018, , .		4
31	A Compact Statistical Model for the Low-Frequency Noise in Halo-Implanted MOSFETs: Large RTN Induced by Halo Implants. IEEE Transactions on Electron Devices, 2019, 66, 3521-3526.	3.0	4
32	Improved Modeling of LDMOS with Non-Uniform Lateral Channel Doping. , 2019, , .		4
33	Simultaneous extraction of threshold voltage and mobility degradation from on-the-fly NBTI measurements. , 2011, , .		3
34	<i>(Invited)</i> Physics and Compact Modeling of SiGe HBT Linearity Using Mextram. ECS Transactions, 2018, 86, 145-154.	0.5	3
35	Compact modeling of noise for RF CMOS circuit simulation. , 2003, , .		2
36	Fast noise prediction for process optimization using only standard DC and S-parameter measurements. , 2012, , .		2

#	ARTICLE	IF	CITATIONS
37	The safe operating volume as a general measure for the operating limits of LDMOS transistors. , 2013, , .		2
38	Identifying failure mechanisms in LDMOS transistors by analytical stability analysis. , 2014, , .		2
39	Improved Compact Modeling of SiGe HBT Linearity With MEXTRAM. IEEE Transactions on Electron Devices, 2021, 68, 2597-2603.	3.0	2
40	Implementation of plug-and-play ESD protection in 5.5GHz 90nm RF CMOS LNAsâ€™ Concepts, constraints and solutions. Microelectronics Reliability, 2006, 46, 702-712.	1.7	1
41	A variability-based analysis technique revealing physical mechanisms of MOSFET low-frequency noise. , 2017, , .		0
42	Foreword Special Issue on Compact Modeling for Circuit Design. IEEE Transactions on Electron Devices, 2019, 66, 7-11.	3.0	0