Shao-Yun Fang

List of Publications by Year
in descending order

35	307	1478505	1281871
35 papers	**307** citations	**6** h-index	**11** g-index
35 all docs	**35** docs citations	**35** times ranked	**171** citing authors

#	Article	IF	Citations
1	COALA: Concurrently Assigning Wire Segments to Layers for 2-D Global Routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 569-582.	2.7	0
2	Demand-Driven Multi-Target Sample Preparation on Resource-Constrained Digital Microfluidic Biochips. ACM Transactions on Design Automation of Electronic Systems, 2022, 27, 1-21.	2.6	1
3	Manufacturability Enhancement With Dummy via Insertion for DSA-MP Lithography Using Multiple BCP Materials. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 400-404.	2.7	1
4	From IC Layout to Die Photograph: A CNN-Based Data-Driven Approach. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 957-970.	2.7	13
5	Placement-guided pin layout substitution for routability optimization. Microelectronics Journal, 2021, 114, 105151.	2.0	0
6	Pin Accessibility Prediction and Optimization With Deep-Learning-Based Pin Pattern Recognition. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2345-2356.	2.7	7
7	Obstacle-Avoiding Open-Net Connector With Precise Shortest Distance Estimation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1096-1108.	2.7	1
8	Stitch-Aware Routing Considering Smart Boundary for Multiple E-Beam Lithography. , 2020, , .		1
9	Obstacle-Avoiding Length-Matching Bus Routing Considering Nonuniform Track Resources. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1881-1892.	3.1	0
10	Pin Accessibility Prediction and Optimization with Deep Learning-based Pin Pattern Recognition. , 2019, , .		23
11	Flip-Chip Routing With I/O Planning Considering Practical Pad Assignment Constraints. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1921-1932.	3.1	3
12	Deep learning-based framework for comprehensive mask optimization. , 2019, , .		5
13	Printability Enhancement with Color Balancing for Multiple Patterning Lithography. IEEE Transactions on Emerging Topics in Computing, 2019, 7, 244-252.	4.6	2
14	Flip-chip routing with IO planning considering practical pad assignment constraints. , 2018, , .		2
15	Provably Good Max–Min- m -Neighbor-TSP-Based Subfield Scheduling for Electron-Beam Photomask Fabrication. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 378-391.	3.1	2
16	Device Array Layout Synthesis With Nonlinear Gradient Compensation for a High-Accuracy Current-Steering DAC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 717-728.	2.7	16
17	RouteNet. , 2018, , .		119
18	PlanarONoC: Concurrent Placement and Routing Considering Crossing Minimization for Optical Networks-on-Chip. , 2018, , .		0

#	Article	IF	Citations
19	Obstacle-Avoiding Open-Net Connector with Precise Shortest Distance Estimation*. , 2018, , .		1
20	Triple patterning lithography-aware detailed routing ensuring via layer decomposability. , 2018, , .		1
21	Guiding Template-Induced Design Challenges in DSA-MP Lithography. , 2018, , .		0
22	Simultaneous Guiding Template Optimization and Redundant via Insertion for Directed Self-Assembly. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 156-169.	2.7	7
23	Guiding template-aware routing considering redundant via insertion for directed self-assembly. , 2017, , .		3
24	Cut Mask Optimization With Wire Planning in Self-Aligned Multiple Patterning Full-Chip Routing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 581-593.	3.1	1
25	Simultaneous template assignment and layout decomposition using multiple bcp materials in DSA-MP lithography. , 2017, , .		7
26	Design Optimization Considering Guiding Template Feasibility and Redundant Via Insertion for Directed Self-Assembly. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 3172-3182.	5.4	0
27	Overlay-aware layout legalization for self-aligned double patterning lithography. , 2016, , .		1
28	Design optimization considering guiding template feasibility and redundant via insertion for directed self-assembly. , 2016, , .		4
29	Trim mask optimization for hybrid multiple pattering lithography. , 2016, , .		1
30	Simultaneous guiding template optimization and redundant via insertion for directed self-assembly. , 2015, , .		11
31	Provably good max-min-m-neighbor-TSP-based subfield scheduling for electron-beam photomask fabrication. , 2015, , .		1
32	Cut mask optimization with wire planning in self-aligned multiple patterning full-chip routing. , 2015, , .		10
33	Stitch-Aware Routing for Multiple E-Beam Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 471-482.	2.7	5
34	A Novel Layout Decomposition Algorithm for Triple Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 397-408.	2.7	50
35	Graph-Based Subfield Scheduling for Electron-Beam Photomask Fabrication. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 189-201.	2.7	8