

Pi-Feng Chiu

List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/796990/publications.pdf>

Version: 2024-02-01

10
papers

207
citations

1937685

4
h-index

1872680

6
g-index

10
all docs

10
docs citations

10
times ranked

238
citing authors

#	ARTICLE	IF	CITATIONS
1	An Agile Approach to Building RISC-V Microprocessors. IEEE Micro, 2016, 36, 8-20.	1.8	79
2	A RISC-V Vector Processor With Simultaneous-Switching Switched-Capacitor DC-DC Converters in 28 nm FDSOI. IEEE Journal of Solid-State Circuits, 2016, 51, 930-942.	5.4	47
3	A RISC-V Processor SoC With Integrated Power Management at Submicrosecond Timescales in 28 nm FD-SOI. IEEE Journal of Solid-State Circuits, 2017, 52, 1863-1875.	5.4	32
4	A RISC-V vector processor with tightly-integrated switched-capacitor DC-DC converters in 28nm FDSOI. , 2015, , .		24
5	A Dual-Core RISC-V Vector Processor With On-Chip Fine-Grain Power Management in 28-nm FD-SOI. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2721-2725.	3.1	7
6	A double-tail sense amplifier for low-voltage SRAM in 28nm technology. , 2016, , .		6
7	An Out-of-Order RISC-V Processor with Resilient Low-Voltage Operation in 28NM CMOS. , 2018, , .		5
8	Reprogrammable Redundancy for SRAM-Based Cache V_{\min} Reduction in a 28-nm RISC-V Processor. IEEE Journal of Solid-State Circuits, 2017, 52, 2589-2600.	5.4	4
9	Cache Resiliency Techniques for a Low-Voltage RISC-V Out-of-Order Processor in 28-nm CMOS. IEEE Solid-State Circuits Letters, 2018, 1, 229-232.	2.0	2
10	Reprogrammable redundancy for cache V_{\min} reduction in a 28nm RISC-V processor. , 2016, , .		1