Rui Liu

List of Publications by Year
in descending order

19 papers	658 citations	933447 10 h-index	1372567 10 g-index
19 all docs	19 docs citations	19 times ranked	779 citing authors

#	Article	IF	Citations
1	Optimizing Weight Mapping and Data Flow for Convolutional Neural Networks on Processing-in-Memory Architectures. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1333-1343.	5.4	47
2	Evaluation of Single Event Effects in SRAM and RRAM Based Neuromorphic Computing System for Inference. , 2019, , .		2
3	Optimizing Weight Mapping and Data Flow for Convolutional Neural Networks on RRAM Based Processing-In-Memory Architecture. , 2019, , .		55
4	MAX^2: An ReRAM-Based Neural Network Accelerator That Maximizes Data Reuse and Area Utilization. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 398-410.	3.6	18
5	Evaluation of Radiation Effects in RRAM-Based Neuromorphic Computing System for Inference. IEEE Transactions on Nuclear Science, 2019, 66, 97-103.	2.0	14
6	XNOR-RRAM: A scalable and parallel resistive synaptic architecture for binary neural networks. , 2018, , .		133
7	X-Point PUF: Exploiting Sneak Paths for a Strong Physical Unclonable Function Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3459-3468.	5.4	16
8	Design and optimization of strong Physical Unclonable Function (PUF) based on RRAM array. , 2017, , .		6
9	Optimization of RRAM-Based Physical Unclonable Function With a Novel Differential Read-Out Method. IEEE Electron Device Letters, 2017, 38, 168-171.	3.9	44
10	Design and optimization of a strong PUF exploiting sneak paths in resistive cross-point array. , 2017, , .		4
11	Low-VDD Operation of SRAM Synaptic Array for Implementing Ternary Neural Network. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2962-2965.	3.1	19
12	Extending 1kb RRAM array from weak PUF to strong PUF by employment of SHA module. , 2017, , .		5
13	A highly reliable and tamper-resistant RRAM PUF: Design and experimental validation. , 2016, , .		36
14	Physical Unclonable Function Exploiting Sneak Paths in Resistive Cross-point Array. IEEE Transactions on Electron Devices, 2016, 63, 3109-3115.	3.0	55
15	Single Event Susceptibility Analysis in CBRAM Resistive Memory Arrays. IEEE Transactions on Nuclear Science, 2015, 62, 2606-2612.	2.0	10
16	Investigation of Single-Bit and Multiple-Bit Upsets in Oxide RRAM-Based 1T1R and Crossbar Memory Arrays. IEEE Transactions on Nuclear Science, 2015, 62, 2294-2301.	2.0	37
17	Scaling 2-layer RRAM cross-point array towards 10 nm node: A device-circuit co-design. , 2015, , .		10
18	Exploiting resistive cross-point array for compact design of physical unclonable function. , 2015, , .		38

#	Article	IF	Citations
19	Experimental Characterization of Physical Unclonable Function Based on 1 kb Resistive Random Access Memory Arrays. IEEE Electron Device Letters, 2015, 36, 1380-1383.	3.9	109