JosÃ© Antonio Rubio Sola

List of Publications by Year
in descending order

106	942	567281 15	642732 23
papers	citations	h-index	g-index

107	107	107	593
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Crossbar-Based Memristive Logic-in-Memory Architecture. IEEE Nanotechnology Magazine, 2017, 16, 491-501.	2.0	57
2	Thermal coupling in integrated circuits: application to thermal testing. IEEE Journal of Solid-State Circuits, 2001, 36, 81-91.	5.4	56
3	Quiescent current sensor circuits in digital VLSI CMOS testing. Electronics Letters, 1990, 26, 1204.	1.0	49
4	Experimental Study of Artificial Neural Networks Using a Digital Memristor Simulator. IEEE Transactions on Neural Networks and Learning Systems, 2018, 29, 5098-5110.	11.3	48
5	Four different approaches for the measurement of IC surface temperature: application to thermal testing. Microelectronics Journal, 2002, 33, 689-696.	2.0	41
6	Experimental comparison of substrate noise coupling using different wafer types. IEEE Journal of Solid-State Circuits, 1999, 34, 1405-1409.	5.4	40
7	A Systematic Method to Design Efficient Ternary High Performance CNTFET-Based Logic Cells. IEEE Access, 2020, 8, 58585-58593.	4.2	35
8	A detailed analysis and electrical modeling of gate oxide shorts in MOS transistors. Journal of Electronic Testing: Theory and Applications (JETTA), 1996, 8, 229-239.	1.2	30
9	Substrate coupling evaluation in BiCMOS technology. IEEE Journal of Solid-State Circuits, 1997, 32, 598-603.	5.4	28
10	An Analysis of Internal Parameter Variations Effects on Nanoscaled Gates. IEEE Nanotechnology Magazine, 2008, 7, 24-33.	2.0	23
11	A Digital Memristor Emulator for FPGA-Based Artificial Neural Networks. , 2016, , .		23
12	Cell architecture for nanoelectronic design. Microelectronics Journal, 2008, 39, 1041-1050.	2.0	22
13	A detailed analysis of CMOS SRAM's with gate oxide short defects. IEEE Journal of Solid-State Circuits, 1997, 32, 1543-1550.	5.4	21
14	Variability and reliability analysis of CNFET technology: Impact of manufacturing imperfections. Microelectronics Reliability, 2015, 55, 358-366.	1.7	21
15	Memristive Logic in Crossbar Memory Arrays: Variability-Aware Design for Higher Reliability. IEEE Nanotechnology Magazine, 2019, 18, 635-646.	2.0	20
16	Analysis of crosstalk interference in CMOS integrated circuits. IEEE Transactions on Electromagnetic Compatibility, 1992, 34, 124-129.	2.2	19
17	Memristive Crossbar Memory Lifetime Evaluation and Reconfiguration Strategies. IEEE Transactions on Emerging Topics in Computing, 2018, 6, 207-218.	4.6	18
18	Circuit propagation delay estimation through multivariate regression-based modeling under spatio-temporal variability. , 2010, , .		16

#	Article	IF	Citations
19	RRAM variability and its mitigation schemes. , 2016, , .		15
20	Built-in dynamic current sensor circuit for digital VLSI CMOS testing. Electronics Letters, 1994, 30, 1668-1669.	1.0	14
21	Fault tolerant structures for nanoscale gates. , 2007, , .		14
22	Localisation of heat sources in electronic circuits by microthermal laser probing. International Journal of Thermal Sciences, 2000, 39, 544-549.	4.9	13
23	Process variability-aware proactive reconfiguration technique for mitigating aging effects in nano scale SRAM lifetime. , 2012, , .		13
24	Power-Efficient Noise-Induced Reduction of ReRAM Cellâ€™s Temporal Variability Effects. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1378-1382.	3.0	13
25	Approach to the analysis of gate oxide shorts in CMOS digital circuits. Microelectronics Reliability, 1992, 32, 1509-1514.	1.7	12
26	Electronic Properties of Graphene Nanoribbons With Defects. IEEE Nanotechnology Magazine, 2021, 20, 151-160.	2.0	12
27	VCTA: A Via-Configurable Transistor Array regular fabric. , 2010, , .		11
28	Crosstalk effects between metal and polysilicon lines in CMOS integrated circuits. IEEE Transactions on Electromagnetic Compatibility, 1994, 36, 250-253.	2.2	10
29	Shape effect on electromigration in VLSI interconnects. Microelectronics Reliability, 1997, 37, 1073-1078.	1.7	10
30	Voltage Divider for Self-Limited Analog State Programing of Memristors. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 620-624.	3.0	10
31	Quasi-adiabatic ternary CMOS logic. Electronics Letters, 1996, 32, 99.	1.0	9
32	Systematic and random variability analysis of two different 6T-SRAM layout topologies. Microelectronics Journal, 2013, 44, 787-793.	2.0	9
33	Probabilistic Resistive Switching Device Modeling Based on Markov Jump Processes. IEEE Access, 2021, 9, 983-988.	4.2	9
34	Impact of FinFET and IIIâ€“V/Ge Technology on Logic and Memory Cell Behavior. IEEE Transactions on Device and Materials Reliability, 2014, 14, 344-350.	2.0	8
35	Iddq secondary components in CMOS logic circuits preceded by defective stages affected by analogue type faults. Electronics Letters, 1991, 27, 1656.	1.0	7
36	Logic testability of defective floating gate CMOS latches. Electronics Letters, 1992, 28, 2305-2306.	1.0	7

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37	Fault localisation in ICs by goniometric laser probing of thermal induced surface waves. Microelectronics Reliability, 1999, 39, 919-923.	1.7	7
38	Applications of temperature phase measurements to IC testing. Microelectronics Reliability, 2004, 44, 95-103.	1.7	7
39	Variability Mitigation Mechanisms in Scaled 3T1D-DRAM Memories to 22 nm and Beyond. IEEE Transactions on Device and Materials Reliability, 2013, 13, 103-109.	2.0	7
40	Adaptive Proactive Reconfiguration: A Technique for Process-Variability- and Aging-Aware SRAM Cache Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1951-1955.	3.1	7
41	Exploring the â€œresistance change per energy unitâ€•as universal performance parameter for resistive switching devices. Solid-State Electronics, 2020, 165, 107748.	1.4	7
42	A VLSI design system for teaching introduction to microelectronics. IEEE Transactions on Education, 1992, 35, 311-320.	2.4	6
43	BiCMOS thermal sensor circuit for built-in test purposes. Electronics Letters, 1998, 34, 1307.	1.0	6
44	Differential Thermal Testing: An Approach to its Feasibility. Journal of Electronic Testing: Theory and Applications (JETTA), 1999, 14, 57-66.	1.2	6
45	A new compensation mechanism for environmental parameter fluctuations in CMOS digital ICs. Microelectronics Journal, 2009, 40, 952-957.	2.0	6
46	Power supply noise and logic error probability. , 2007, , .		5
47	Effectiveness of hybrid recovery techniques on parametric failures. , 2013, , .		5
48	Experimental Time Evolution Study of the HfO₂-Based IMPLY Gate Operation. IEEE Transactions on Electron Devices, 2018, 65, 404-410.	3.0	5
49	Active Radiation-Hardening Strategy in Bulk FinFETs. IEEE Access, 2020, 8, 201441-201449.	4.2	5
50	Built-in dynamic thermal testing technique for ICs. Electronics Letters, 1996, 32, 1982.	1.0	4
51	Measurement of crosstalk-induced delay errors in integrated circuits. Electronics Letters, 1997, 33, 1623.	1.0	4
52	Error probability in synchronous digital circuits due to power supply noise. , 2007, , .		4
53	Manufacturing variability analysis in Carbon Nanotube Technology: A comparison with bulk CMOS in 6T SRAM scenario. , 2011, , .		4
54	Adaptive Fault-Tolerant Architecture for Unreliable Technologies With Heterogeneous Variability. IEEE Nanotechnology Magazine, 2012, 11, 818-829.	2.0	4

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55	Impact of FinFET Technology Introduction in the 3T1D-DRAM Memory Cell. IEEE Transactions on Device and Materials Reliability, 2013, 13, 287-292.	2.0	4
56	Statistical Analysis and Comparison of 2T and 3T1D e-DRAM Minimum Energy Operation. IEEE Transactions on Device and Materials Reliability, 2017, 17, 42-51.	2.0	4
57	An investigation on the relation between digital circuitry characteristics and power supply noise spectrum in mixed-signal CMOS integrated circuits. Microelectronics Journal, 2005, 36, 77-84.	2.0	3
58	Turtle Logic: A new probabilistic design methodology of nanoscale digital circuits. , 2010, , .		3
59	Carbon nanotube growth process-related variability in CNFETs. , 2011, , .		3
60	New redundant logic design concept for high noise and low voltage scenarios. Microelectronics Journal, 2011, 42, 1359-1369.	2.0	3
61	Degradation Stochastic Resonance (DSR) in AD-AVG architectures. , 2012, , .		3
62	Impact of positive bias temperature instability (PBTI) on 3T1D-DRAM cells. The Integration VLSI Journal, 2012, 45, 246-252.	2.1	3
63	Novel redundant logic design for noisy low voltage scenarios. , 2013, , .		3
64	Monitoring SRAM BTI degradation by current-based tracking technique. , 2016, , .		3
65	An on-line test strategy and analysis for a 1T1R crossbar memory. , 2017, , .		3
66	Experimental Verification of Memristor-Based Material Implication NAND Operation. IEEE Transactions on Emerging Topics in Computing, 2019, 7, 545-552.	4.6	3
67	A Pragmatic Gaze on Stochastic Resonance Based Variability Tolerant Memristance Enhancement. , 2019, , .		3
68	Resistive Random Access Memory Variability and Its Mitigation Schemes. Journal of Low Power Electronics, 2017, 13, 124-134.	0.6	3
69	Design of easily testable iterative systems. Microprocessing and Microprogramming, 1987, 20, 141-146.	0.2	2
70	Off-chip Iddq monitor with standard test interface. Electronics Letters, 1995, 31, 1139.	1.0	2
71	Ground bounce modelling for digital gigascale integrated circuits. International Journal of Electronics, 2008, 95, 227-237.	1.4	2
72	Controlled Degradation Stochastic Resonance in Adaptive Averaging Cell-Based Architectures. IEEE Nanotechnology Magazine, 2013, 12, 888-896.	2.0	2

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73	Reliability and Performance Tunable Architecture: The Partially Asynchronous R-Fold Modular Redundancy (pA-RMR). IEEE Nanotechnology Magazine, 2014, 13, 617-622.	2.0	2
74	Impact of adaptive proactive reconfiguration technique on Vmin and lifetime of SRAM caches. , 2014, , .		2
75	Insights to memristive memory cell from a reliability perspective. , 2015, , .		2
76	Analysis and design of an adaptive proactive reconfiguration approach for memristive crossbar memories. , 2015, , .		2
77	Reliability issues in RRAM ternary memories affected by variability and aging mechanisms. , 2017, , .		2
78	Shortest Path Computing in Directed Graphs with Weighted Edges Mapped on Random Networks of Memristors. Parallel Processing Letters, 2020, 30, 2050002.	0.6	2
79	Analysis of spurious signal propagation in digital CMOS circuits. International Journal of Electronics, 1992, 73, 621-625.	1.4	1
80	Adaptive fault-tolerant architecture for unreliable device technologies. , 2011, , .		1
81	A comparative variability analysis for CMOS and CNFET 6T SRAM cells. , 2011, , .		1
82	Impact of bulk/SOI 10nm FinFETs on 3T1D-DRAM cell performance. , 2012, , .		1
83	Fault-tolerant nanoscale architecture based on linear threshold gates with redundancy. Microprocessors and Microsystems, 2012, 36, 420-426.	2.8	1
84	Suitability of the FinFET 3T1D Cell Beyond 10 nm. IEEE Nanotechnology Magazine, 2014, 13, 926-932.	2.0	1
85	An experience with chalcogenide memristors, and implications on memory and computer applications. , 2016, , .		1
86	Analysis of Body Bias and RTN-Induced Frequency Shift of Low Voltage Ring Oscillators in FDSOI Technology. , 2018, , .		1
87	Stuck-at-OFF Fault Analysis in Memristor-Based Architecture for Synchronization. , 2019, , .		1
88	Noise-induced Performance Enhancement of Variability-aware Memristor Networks. , 2019, , .		1
89	A mechanism for detection and recovery from transient failures in industrial controllers. Microprocessing and Microprogramming, 1985, 15, 11-15.	0.2	0
90	Advanced failure detection techniques in deep submicron CMOS integrated circuits. Microelectronics Reliability, 1999, 39, 909-918.	1.7	0

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91	A new probabilistic design methodology of nanoscale digital circuits. , 2011, , .		0
92	TRAMS Project: Variability and Reliability of SRAM Memories in sub-22nm Bulk-CMOS Technologies. Procedia Computer Science, 2011, 7, 148-149.	2.0	0
93	Design of complex circuits using the Via-Configurable transistor array regular layout fabric. , 2011, , .		0
94	Design and Implementation of an Adaptive Proactive Reconfiguration Technique for SRAM Caches. , 2013, , .		0
95	Study on the optimal distribution of redundancy effort in cross-layer reliable architectures. , 2013, , .		0
96	Guest Editors' Introduction: Special Issue on Variability and Aging. IEEE Design and Test, 2013, 30, 5-7.	1.2	0
97	A shapeshifting evolvable hardware mechanism based on reconfigurable memFETs crossbar architecture. Microelectronics Reliability, 2014, 54, 1500-1510.	1.7	0
98	Memristive crossbar design and test in non-adaptive proactive reconfiguring scheme. , 2015, , .		0
99	Heterogeneous memristive crossbar for in-memory computing. , 2015, , .		0
100	Optimization of FinFET-Based Gain Cells for Low Power Sub-V_T Embedded DRAMs. Journal of Low Power Electronics, 2018, 14, 236-243.	0.6	0
101	Transition Activity Estimation for Digital Signal Processing Systems. Journal of Low Power Electronics, 2005, 1, 217-225.	0.6	0
102	The cause of switching noise. , 1999, , 143-169.		0
103	Variability Influence on FinFET-Based On-Chip Memory Data Paths. Journal of Low Power Electronics, 2015, 11, 250-255.	0.6	0
104	A Memristor-based Quaternary Memory with Adaptive Noise Tolerance. , 2020, , .		0
105	Ubiquitous memristors on-chip in multi-level memory, in-memory computing, data converters, clock generation and signal transmission. , 2022, , 445-463.		0
106	Influence of Punch Trough Stop Layer and Well Depths on the Robustness of Bulk FinFETs to Heavy Ions Impact. IEEE Access, 2022, 10, 47169-47178.	4.2	0