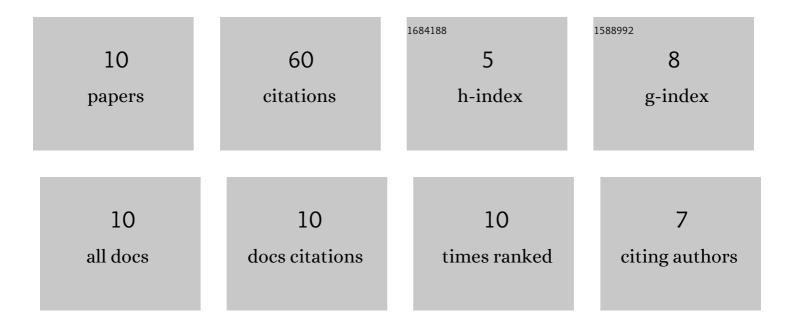
## Zhenshan Xie

List of Publications by Year in descending order

Source: https://exaly.com/author-pdf/7944473/publications.pdf Version: 2024-02-01



7HENSHAN XIE

#	Article	IF	CITATIONS
1	Efficient Architectures for Generalized Integrated Interleaved Decoder. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4018-4031.	5.4	16
2	Reduced-Complexity Key Equation Solvers for Generalized Integrated Interleaved BCH Decoders. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 5520-5529.	5.4	9
3	Scaled Nested Key Equation Solver for Generalized Integrated Interleaved Decoder. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2457-2461.	3.0	8
4	Miscorrection Mitigation for Generalized Integrated Interleaved BCH Codes. IEEE Communications Letters, 2021, 25, 2118-2122.	4.1	8
5	Fast Nested Key Equation Solvers for Generalized Integrated Interleaved Decoder. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 483-495.	5.4	7
6	Relaxing the Constraints on Locally Recoverable Erasure Codes by Finite Field Element Variation. IEEE Communications Letters, 2019, 23, 1680-1683.	4.1	5
7	Scaled Fast Nested Key Equation Solver for Generalized Integrated Interleaved BCH Decoders. , 2021, , .		3
8	Efficient Sub-Codeword Key Equation Solver for Generalized Integrated Interleaved BCH Decoder. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 85-89.	3.0	2
9	Efficient VLSI Architectures for Coupled-Layered Regenerating Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1869-1873.	3.0	1
10	Low-Latency Nested Decoding for Short Generalized Integrated Interleaved BCH Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1563-1567.	3.1	1