M Jagadesh Kumar

List of Publications by Year in Descending Order

201 papers	5,044 citations	37 h-index	64 g-index
250 ext. papers	6,109 ext. citations	2.2 avg, IF	6.59 L-index

#	Paper	IF	Citations
201	What is in store in the March-April 2021 issue of IETE Technical Review?. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2021**, 38, 195-196	1.5	
200	Reconfigurable FET Biosensor for a Wide Detection Range and Electrostatically Tunable Sensing Response. *IEEE Sensors Journal*, **2020**, 20, 2261-2269	4	13
199	Sub-10 nm Scalability of Junctionless FETs Using a Ground Plane in High-K BOX: A Simulation Study. *IEEE Access*, **2020**, 8, 137540-137548	3.5	7
198	. *IEEE Transactions on Electron Devices*, **2019**, 66, 3209-3214	2.9	12
197	A Line Tunneling Field-Effect Transistor Based on Misaligned Core‐Shell Gate Architecture in Emerging Nanotube FETs. *IEEE Transactions on Electron Devices*, **2019**, 66, 2809-2816	2.9	32
196	Gate-Induced Drain Leakage in Junctionless Field-Effect Transistors **2019**, 173-254		
195	Junctionless Devices Without Any Chemical Doping **2019**, 281-325		3
194	Introduction to Field-Effect Transistors **2019**, 1-26		
193	Conclusion and Perspectives **2019**, 439-456		
192	Emerging Fet Architectures **2019**, 27-66		0
191	Fundamentals of Junctionless Field-Effect Transistors **2019**, 67-123		0
190	Device Architectures to Mitigate Challenges in Junctionless Field-Effect Transistors **2019**, 125-172		1
189	Impact Ionization in Junctionless Field-Effect Transistors **2019**, 255-279		
188	Modeling Junctionless Field-Effect Transistors **2019**, 327-384		3
187	Simulation of JLFETS Using Sentaurus TCAD **2019**, 385-438		0
186	Investigation of the Scalability of Emerging Nanotube Junctionless FETs Using an Intrinsic Pocket. *IEEE Journal of the Electron Devices Society*, **2019**, 7, 888-896	2.3	6
185	Nanotube Tunneling FET With a Core Source for Ultrasteep Subthreshold Swing: A Simulation Study. *IEEE Transactions on Electron Devices*, **2019**, 66, 4425-4432	2.9	33

184	**2019**,		38
183	An Impact Ionization MOSFET With Reduced Breakdown Voltage Based on Back-Gate Misalignment. *IEEE Transactions on Electron Devices*, **2019**, 66, 868-875	2.9	6
182	A New On-Chip ESD Strategy Using TFETs-TCAD Based Device and Network Simulations. *IEEE Journal of the Electron Devices Society*, **2018**, 6, 298-308	2.3	7
181	Controlling L-BTBT in Emerging Nanotube FETs Using Dual-Material Gate. *IEEE Journal of the Electron Devices Society*, **2018**, 6, 611-621	2.3	25
180	1-T Capacitorless DRAM Using Laterally Bandgap Engineered Si-Si:C Heterostructure Bipolar I-MOS for Improved Sensing Margin and Retention Time. *IEEE Nanotechnology Magazine*, **2018**, 17, 543-551	2.6	4
179	Charge Plasma High Voltage PIN Diode Investigation **2018**,		2
178	Diameter Dependence of Leakage Current in Nanowire Junctionless Field Effect Transistors. *IEEE Transactions on Electron Devices*, **2017**, 64, 1330-1335	2.9	67
177	1-T Capacitorless DRAM Using Bandgap-Engineered Silicon-Germanium Bipolar I-MOS. *IEEE Transactions on Electron Devices*, **2017**, 64, 1583-1590	2.9	16
176	Schottky bipolar I-MOS: An I-MOS with Schottky electrodes and an open-base BJT configuration for reduced operating voltage. *Superlattices and Microstructures*, **2017**, 104, 422-427	2.8	3
175	Nanotube Junctionless FET: Proposal, Design, and Investigation. *IEEE Transactions on Electron Devices*, **2017**, 64, 1851-1856	2.9	76
174	. *IEEE Transactions on Electron Devices*, **2017**, 64, 21-27	2.9	33
173	A Tunnel Dielectric-Based Junctionless Transistor With Reduced Parasitic BJT Action. *IEEE Transactions on Electron Devices*, **2017**, 64, 3470-3475	2.9	14
172	Spacer Design Guidelines for Nanowire FETs From Gate-Induced Drain Leakage Perspective. *IEEE Transactions on Electron Devices*, **2017**, 64, 3007-3015	2.9	40
171	DC Drain Current Model for Tunnel FETs Considering Source and Drain Depletion Regions **2017**,		1
170	Physical Insights Into the Nature of Gate-Induced Drain Leakage in Ultrashort Channel Nanowire FETs. *IEEE Transactions on Electron Devices*, **2017**, 64, 2604-2610	2.9	41
169	Comprehensive Analysis of Gate-Induced Drain Leakage in Emerging FET Architectures: Nanotube FETs Versus Nanowire FETs. *IEEE Access*, **2017**, 5, 18918-18926	3.5	26
168	In0.53Ga0.47As/InP Trench-Gate Power MOSFET Based on Impact Ionization for Improved Performance: Design and Analysis. *IEEE Transactions on Electron Devices*, **2017**, 64, 4561-4567	2.9	4
167	The Charge Plasma n-p-n Impact Ionization MOS on FDSOI Technology: Proposal and Analysis. *IEEE Transactions on Electron Devices*, **2017**, 64, 3-7	2.9	9

166	. *IEEE Transactions on Electron Devices*, **2017**, 64, 4430-4434	2.9	21
165	Thin Capacitively-Coupled Thyristor as an Ultrasensitive Label-Free Nanogap Biosensor: Proposal and Investigation **2017**, 1, 1-4		1
164	Schottky Barrier FET Biosensor for Dual Polarity Detection: A Simulation Study. *IEEE Electron Device Letters*, **2017**, 38, 1594-1597	4.4	8
163	Double gate symmetric tunnel FET: investigation and analysis. *IET Circuits, Devices and Systems*, **2017**, 11, 365-370	1.1	16
162	Controlling L-BTBT and Volume Depletion in Nanowire JLFETs Using Core–Shell Architecture. *IEEE Transactions on Electron Devices*, **2016**, 63, 3790-3794	2.9	53
161	Insight into Lateral Band-to-Band-Tunneling in Nanowire Junctionless FETs. *IEEE Transactions on Electron Devices*, **2016**, 63, 4138-4142	2.9	64
160	A Novel Gate-Stack-Engineered Nanowire FET for Scaling to the Sub-10-nm Regime. *IEEE Transactions on Electron Devices*, **2016**, 63, 5055-5059	2.9	39
159	Controlling BTBT-Induced Parasitic BJT Action in Junctionless FETs Using a Hybrid Channel. *IEEE Transactions on Electron Devices*, **2016**, 63, 3350-3353	2.9	47
158	Realizing Efficient Volume Depletion in SOI Junctionless FETs. *IEEE Journal of the Electron Devices Society*, **2016**, 4, 110-115	2.3	55
157	. *IEEE Transactions on Device and Materials Reliability*, **2016**, 16, 200-207	1.6	4
156	Modeling a Dual-Material-Gate Junctionless FET Under Full and Partial Depletion Conditions Using Finite-Differentiation Method. *IEEE Transactions on Electron Devices*, **2016**, 63, 2282-2287	2.9	10
155	Raised Source/Drain Dopingless Junctionless Accumulation Mode FET: Design and Analysis. *IEEE Transactions on Electron Devices*, **2016**, 63, 4185-4190	2.9	14
154	Dielectric-Modulated Field Effect Transistors for DNA Detection: Impact of DNA Orientation. *IEEE Electron Device Letters*, **2016**, 37, 1485-1488	4.4	31
153	2-D Threshold Voltage Model for the Double-Gate p-n-p-n TFET With Localized Charges. *IEEE Transactions on Electron Devices*, **2016**, 63, 3663-3668	2.9	20
152	A full-range dual material gate tunnel field effect transistor drain current model considering both source and drain depletion region band-to-band tunneling. *Journal of Computational Electronics*, **2015**, 14, 280-287	1.8	29
151	An Accurate Compact Analytical Model for the Drain Current of a TFET From Subthreshold to Strong Inversion. *IEEE Transactions on Electron Devices*, **2015**, 62, 478-484	2.9	36
150	PNPN tunnel FET with controllable drain side tunnel barrier width: Proposal and analysis. *Superlattices and Microstructures*, **2015**, 86, 121-125	2.8	27
149	Dielectric modulated overlapping gate-on-drain tunnel-FET as a label-free biosensor. *Superlattices and Microstructures*, **2015**, 86, 198-202	2.8	58

148	Junctionless Biristor: A Bistable Resistor Without Chemically Doped P-N Junctions. *IEEE Journal of the Electron Devices Society*, **2015**, 3, 311-315	2.3	15
147	Investigation of laterally single-diffused metal oxide semiconductor (LSMOS) field effect transistor. *Current Applied Physics*, **2015**, 15, 1130-1133	2.6	9
146	Charge-Modulated Underlap I-MOS Transistor as a Label-Free Biosensor: A Simulation Study. *IEEE Transactions on Electron Devices*, **2015**, 62, 2645-2651	2.9	30
145	A Silicon Biristor With Reduced Operating Voltage: Proposal and Analysis. *IEEE Journal of the Electron Devices Society*, **2015**, 3, 67-72	2.3	13
144	The Pay or Perish Game: Why we should stand up against ﬁctive discrimination for the survival of net neutrality. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2015**, 32, 161-163	1.5	
143	Controlling the Drain Side Tunneling Width to Reduce Ambipolar Current in Tunnel FETs Using Heterodielectric BOX. *IEEE Transactions on Electron Devices*, **2015**, 62, 3882-3886	2.9	93
142	Bipolar I-MOS: An Impact-Ionization MOS With Reduced Operating Voltage Using the Open-Base BJT Configuration. *IEEE Transactions on Electron Devices*, **2015**, 62, 4345-4348	2.9	20
141	Smart Cities with Massive Data Centric Living are Hard to Build Without 5G Networks. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2015**, 32, 237-239	1.5	4
140	GaAs Tunnel Diode With Electrostatically Doped n-Region: Proposal and Analysis. *IEEE Transactions on Electron Devices*, **2015**, 62, 3445-3448	2.9	9
139	Schottky Biristor: A Metal-Semiconductor-Metal Bistable Resistor. *IEEE Transactions on Electron Devices*, **2015**, 62, 2360-2363	2.9	13
138	Global University Rankings: What should India do?. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2015**, 32, 81-83	1.5	2
137	A pseudo 2-D surface potential model of a dual material double gate junctionless field effect transistor. *Journal of Computational Electronics*, **2015**, 14, 686-693	1.8	9
136	Innovation and Technology should Lead to Abundance not Scarcity. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2015**, 32, 1-2	1.5	11
135	A Compact Analytical Model for the drain current of a TFET with non-abrupt doping profile incorporating the effect of band-gap narrowing **2015**,		1
134	Two dimensional analytical model for the threshold voltage of a Gate All Around Nanowire tunneling FET with localized charges **2015**,		1
133	A Compact Analytical Model for the Drain Current of Gate-All-Around Nanowire Tunnel FET Accurate From Sub-Threshold to ON-State. *IEEE Nanotechnology Magazine*, **2015**, 14, 358-362	2.6	21
132	Vertical bipolar charge plasma transistor with buried metal layer. *Scientific Reports*, **2015**, 5, 7860	4.9	27
131	Compact Analytical Model of Dual Material Gate Tunneling Field-Effect Transistor Using Interband Tunneling and Channel Transport. *IEEE Transactions on Electron Devices*, **2014**, 61, 1936-1942	2.9	81

130	Controlling the ON-resistance in SOI LDMOS using parasitic bipolar junction transistor. *Journal of Computational Electronics*, **2014**, 13, 857-861	1.8	2
129	Compact Analytical Drain Current Model of Gate-All-Around Nanowire Tunneling FET. *IEEE Transactions on Electron Devices*, **2014**, 61, 2599-2603	2.9	72
128	A Pseudo-2-D-Analytical Model of Dual Material Gate All-Around Nanowire Tunneling FET. *IEEE Transactions on Electron Devices*, **2014**, 61, 2264-2270	2.9	53
127	In-Built N+ Pocket p-n-p-n Tunnel Field-Effect Transistor. *IEEE Electron Device Letters*, **2014**, 35, 1170-1172	4.4	95
126	2-D Analytical Model for the Threshold Voltage of a Tunneling FET With Localized Charges. *IEEE Transactions on Electron Devices*, **2014**, 61, 3054-3059	2.9	34
125	Junctionless Impact Ionization MOS: Proposal and Investigation. *IEEE Transactions on Electron Devices*, **2014**, 61, 4295-4298	2.9	44
124	Thin-Film Bipolar Transistors on Recrystallized Polycrystalline Silicon Without Impurity Doped Junctions: Proposal and Investigation. *Journal of Display Technology*, **2014**, 10, 590-594		34
123	Impact of gate leakage considerations in tunnel field effect transistor design. *Japanese Journal of Applied Physics*, **2014**, 53, 074201	1.4	16
122	We are Expanding the Editorial Board. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2014**, 31, 307-307	1.5	
121	Controlling Ambipolar Current in Tunneling FETs Using Overlapping Gate-on-Drain. *IEEE Journal of the Electron Devices Society*, **2014**, 2, 187-190	2.3	193
120	Facing the Students on Facebook: Are You Game for It?. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2014**, 31, 115-117	1.5	1
119	Numerical study of the threshold voltage of TFETs with localized charges **2014**,		1
118	Drain current model for SOI TFET considering source and drain side tunneling **2014**,		6
117	Expanding the Boundaries of Your Research Using Social Media: Stand-Up and Be Counted. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2014**, 31, 255-257	1.5	7
116	Telling Lies to Describe Truth: Do we Emphasize the Importance of The Art of Approximations to the Students?. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2014**, 31, 1-3	1.5	1
115	Quantum Computing in India: An Opportunity that Should Not Be Missed. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2014**, 31, 187-189	1.5	
114	A dc model for partially depleted SOI laterally diffused MOSFETs utilizing the HiSIM-HV compact model. *Journal of Computational Electronics*, **2013**, 12, 460-468	1.8	2
113	Doping-Less Tunnel Field Effect Transistor: Design and Investigation. *IEEE Transactions on Electron Devices*, **2013**, 60, 3285-3290	2.9	376

112	Dielectric-Modulated Impact-Ionization MOS Transistor as a Label-Free Biosensor. *IEEE Electron Device Letters*, **2013**, 34, 1575-1577	4.4	87
111	Face Recognition by Machines: Is It an Effective Surveillance Tactic?. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2013**, 30, 93	1.5	2
110	How does the power of "Suggestion" influence students? performance?. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2013**, 30, 273	1.5	
109	Making Your Research Paper Discoverable: Title Plays the Winning Trick. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2013**, 30, 361	1.5	5
108	Schottky Collector Bipolar Transistor Without Impurity Doped Emitter and Base: Design and Performance. *IEEE Transactions on Electron Devices*, **2013**, 60, 2956-2959	2.9	37
107	The Malady of Technology in Our Lives: Is Anyone Listening?. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2013**, 30, 3	1.5	2
106	Back to Basics: Why Every Student and Professor Should Ride a Bicycle on a University Campus?. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2013**, 30, 165	1.5	
105	Bipolar Charge-Plasma Transistor: A Novel Three Terminal Device. *IEEE Transactions on Electron Devices*, **2012**, 59, 962-967	2.9	152
104	Controlled deposition of aligned carbon nanotubes by floating electrodes dielectrophoresis **2012**,		1
103	Honestly speaking about academic dishonesty. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2012**, 29, 357	1.5	3
102	. *IEEE Transactions on Electron Devices*, **2012**, 59, 738-744	2.9	17
101	Improving the breakdown voltage, ON-resistance and gate-charge of InGaAs LDMOS power transistors. *Semiconductor Science and Technology*, **2012**, 27, 105030	1.8	15
100	Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field-Effect Transistor. *IEEE Transactions on Electron Devices*, **2011**, 58, 404-410	2.9	289
99	. *IEEE Transactions on Electron Devices*, **2011**, 58, 3485-3493	2.9	6
98	**2011**,		6
97	Reflections on Teaching a Large Class. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2011**, 28, 275	1.5	
96	Estimation and Compensation of Process-Induced Variations in Nanoscale Tunnel Field-Effect Transistors for Improved Reliability. *IEEE Transactions on Device and Materials Reliability*, **2010**, 10, 390-395	1.6	50
95	Linearity and speed optimization in SOI LDMOS using gate engineering. *Semiconductor Science and Technology*, **2010**, 25, 015006	1.8	12

94	A New Hetero-material Stepped Gate (HSG) SOI LDMOS for RF Power Amplifier Applications **2010**,		3
93	. *IEEE Transactions on Electron Devices*, **2010**, 57, 7-11	2.9	2
92	Extended-$hbox{p}^{+}$ Stepped Gate LDMOS for Improved Performance. *IEEE Transactions on Electron Devices*, **2010**, 57, 1719-1724	2.9	51
91	Dual-Material-Gate Technique for Enhanced Transconductance and Breakdown Voltage of Trench Power MOSFETs. *IEEE Transactions on Electron Devices*, **2009**, 56, 517-522	2.9	30
90	A Stepped Oxide Hetero-Material Gate Trench Power MOSFET for Improved Performance. *IEEE Transactions on Electron Devices*, **2009**, 56, 1355-1359	2.9	27
89	Recessed source concept in nanoscale vertical surrounding gate (VSG) MOSFETs for controlling short-channel effects. *Physica E: Low-Dimensional Systems and Nanostructures*, **2009**, 41, 671-676	3	10
88	A New Buried-Oxide-In-Drift-Region Trench MOSFET With Improved Breakdown Voltage. *IEEE Electron Device Letters*, **2009**, 30, 990-992	4.4	6
87	Memristor - Why Do We Have to Know About It?. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2009**, 26, 3	1.5	13
86	Impact of Strain on Drain Current and Threshold Voltage of Nanoscale Double Gate Tunnel Field Effect Transistor: Theoretical Investigation and Analysis. *Japanese Journal of Applied Physics*, **2009**, 48, 064503	1.4	93
85	Evaluating Scientists: Citations, Impact Factor, h-Index, Online Page Hits and What Else?. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2009**, 26, 165	1.5	13
84	Analytical drain current model for nanoscale strained-Si/SiGe MOSFETs. *COMPEL - the International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, **2009**, 28, 353-371	0.7	13
83	A new SiGe Stepped Gate (SSG) thin film SOI LDMOS for enhanced breakdown voltage and reduced delay **2009**,		2
82	Compact Surface Potential Model for FD SOI MOSFET Considering Substrate Depletion Region. *IEEE Transactions on Electron Devices*, **2008**, 55, 789-795	2.9	19
81	A New Strained-Silicon Channel Trench-Gate Power MOSFET: Design and Analysis. *IEEE Transactions on Electron Devices*, **2008**, 55, 3299-3304	2.9	16
80	. *IEEE Transactions on Electron Devices*, **2008**, 55, 2813-2819	2.9	6
79	The Ground Plane in Buried Oxide for Controlling Short-Channel Effects in Nanoscale SOI MOSFETs. *IEEE Transactions on Electron Devices*, **2008**, 55, 1554-1557	2.9	43
78	Guest Editorial Special Issue on Nanowire Transistors: Modeling, Device Design, and Technology. *IEEE Nanotechnology Magazine*, **2008**, 7, 643-650	2.6	2
77	Being Wary of Plagiarism. *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, **2008**, 25, 231	1.5	

76	QUANTUM CONFINEMENT EFFECTS IN STRAINED SILICON MOSFETS. *International Journal of Nanoscience*, **2008**, 07, 81-84	0.6	15
75	Effect of the Ge mole fraction on the formation of a conduction path in cylindrical strained-silicon-on-SiGe MOSFETs. *Superlattices and Microstructures*, **2008**, 44, 79-85	2.8	14
74	Approaches to nanoscale MOSFET compact modeling using surface potential based models **2007**,		1
73	. *IEEE Transactions on Electron Devices*, **2007**, 54, 554-562	2.9	35
72	Comprehensive approach to modeling threshold voltage of nanoscale strained silicon SOI MOSFETs. *Journal of Computational Electronics*, **2007**, 6, 439-444	1.8	11
71	Molecular diodes and applications. *Recent Patents on Nanotechnology*, **2007**, 1, 51-7	1.2	19
70	Analytical Drain Current Model of Nanoscale Strained-Si/SiGe MOSFETs for Analog Circuit Simulation **2007**,		3
69	Impact of Strain or Ge Content on the Threshold Voltage of Nanoscale Strained-Si/SiGe Bulk MOSFETs. *IEEE Transactions on Device and Materials Reliability*, **2007**, 7, 181-187	1.6	29
68	Nanoscale SOI MOSFETs with electrically induced source/drain extension: Novel attributes and design considerations for suppressed short-channel effects. *Superlattices and Microstructures*, **2006**, 39, 395-405	2.8	16
67	A super beta bipolar transistor using SiGe-base surface accumulation layer transistor(SALTran) concept: a simulation study. *IEEE Transactions on Electron Devices*, **2006**, 53, 577-579	2.9	13
66	New dual-material SG nanoscale MOSFET: analytical threshold-voltage model. *IEEE Transactions on Electron Devices*, **2006**, 53, 920-922	2.9	58
65	Compact modeling of the effects of parasitic internal fringe capacitance on the threshold voltage of high-k gate-dielectric nanoscale SOI MOSFETs. *IEEE Transactions on Electron Devices*, **2006**, 53, 706-711	2.9	31
64	New Schottky-Gate Bipolar-Mode Field-Effect Transistor (SBMFET): Design and Analysis Using Two-Dimensional Simulation. *IEEE Transactions on Electron Devices*, **2006**, 53, 2364-2369	2.9	1
63	. *IEEE Transactions on Electron Devices*, **2006**, 53, 2500-2506	2.9	37
62	A new grounded lamination gate (GLG) for diminished fringe-capacitance effects in high-/spl kappa/ gate-dielectric MOSFETs. *IEEE Transactions on Electron Devices*, **2006**, 53, 2578-2581	2.9	1
61	New Silicon Carbide Schottky-gate Bipolar Mode Field Effect Transistor (SiC SBMFET) without PN Junction **2006**,		2
60	Leakage current reduction techniques in poly-Si TFTs for active matrix liquid crystal displays: a comprehensive study. *IEEE Transactions on Device and Materials Reliability*, **2006**, 6, 315-325	1.6	31
59	. *IEEE Transactions on Device and Materials Reliability*, **2006**, 6, 306-314	1.6	7

58	A New Gate Induced Barrier Thin-Film Transistor (GIB-TFT) for Active Matrix Liquid Crystal Displays: Design and Performance Considerations. *Journal of Display Technology*, **2006**, 2, 372-377		1
57	Silicon-on-insulator lateral dual sidewall Schottky (SOI-LDSS) concept for improved rectifier performance: a two-dimensional simulation study. *Microelectronics International*, **2006**, 23, 16-18	0.8	
56	Investigation of a new modified source/drain for diminished self-heating effects in nanoscale MOSFETs using computer simulation. *Physica E: Low-Dimensional Systems and Nanostructures*, **2006**, 33, 134-138	3	29
55	Enhanced breakdown voltage and reduced self-heating effects in thin-film lateral bipolar transistors: Design and analysis using 2-D simulation. *Microelectronic Engineering*, **2006**, 83, 303-311	2.5	1
54	A new symmetrical double gate nanoscale MOSFET with asymmetrical side gates for electrically induced source/drain. *Microelectronic Engineering*, **2006**, 83, 409-414	2.5	16
53	Development of a Monte Carlo Simulation Suite for Predicting the Electron Beam Interaction with Resist on Semiconductor Substrates. *IETE Journal of Research*, **2005**, 51, 301-309	0.9	
52	Shielded channel double-gate MOSFET: a novel device for reliable nanoscale CMOS applications. *IEEE Transactions on Device and Materials Reliability*, **2005**, 5, 509-514	1.6	26
51	The Simulation of a new asymmetrical double-gate poly-Si TFT with modified channel conduction mechanism for highly reduced OFF-state leakage current. *IEEE Transactions on Device and Materials Reliability*, **2005**, 5, 675-682	1.6	3
50	A new dual-material double-gate (DMDG) nanoscale SOI MOSFET-two-dimensional analytical modeling and simulation. *IEEE Nanotechnology Magazine*, **2005**, 4, 260-268	2.6	158
49	Realizing high-voltage thin film lateral bipolar transistors on SOI with a collector-tub. *Microelectronics International*, **2005**, 22, 3-9	0.8	6
48	Realising high-current gain p-n-p transistors using a novel surface accumulation layer transistor (SALTran) concept. *IET Circuits, Devices and Systems*, **2005**, 152, 178		3
47	Two-dimensional analytical threshold voltage model of nanoscale fully depleted SOI MOSFET with electrically induced S/D extensions. *IEEE Transactions on Electron Devices*, **2005**, 52, 1568-1575	2.9	51
46	On the parasitic gate capacitance of small-geometry MOSFETs. *IEEE Transactions on Electron Devices*, **2005**, 52, 1676-1677	2.9	4
45	A new poly-Si TG-TFT with diminished pseudosubthreshold region: theoretical investigation and analysis. *IEEE Transactions on Electron Devices*, **2005**, 52, 1815-1820	2.9	11
44	A new high breakdown voltage lateral Schottky collector bipolar transistor on SOI: design and analysis. *IEEE Transactions on Electron Devices*, **2005**, 52, 2496-2501	2.9	12
43	Enhanced current gain in SiC power BJTs using a novel surface accumulation layer transistor concept. *Microelectronic Engineering*, **2005**, 81, 90-95	2.5	5
42	ShOC rectifier: a new metal-semiconductor device with excellent forward and reverse characteristics. *IEEE Transactions on Electron Devices*, **2005**, 52, 130-132	2.9	7
41	Diminished Short Channel Effects in Nanoscale Double-Gate Silicon-on-Insulator Metal□Oxide□Semiconductor Field-Effect-Transistors due to Induced Back-Gate Step Potential. *Japanese Journal of Applied Physics*, **2005**, 44, 6508-6509	1.4	18

40	Inverse modeling of delta doped pseudomorphic high electron mobility transistors. *Journal of Vacuum Science and Technology A: Vacuum, Surfaces and Films*, **2004**, 22, 1036	2.9	1
39	Proposal and design of a new SiC-emitter lateral NPM Schottky collector bipolar transistor on SOI for VLSI applications. *IET Circuits, Devices and Systems*, **2004**, 151, 63		4
38	Realising wide bandgap P-SiC-emitter lateral heterojunction bipolar transistors with low collector–emitter offset voltage and high current gain: a novel proposal using numerical simulation. *IET Circuits, Devices and Systems*, **2004**, 151, 399		7
37	Two-dimensional analytical modeling of fully depleted DMG SOI MOSFET and evidence for diminished SCEs. *IEEE Transactions on Electron Devices*, **2004**, 51, 569-574	2.9	198
36	Investigation of the novel attributes of a fully depleted dual-material gate SOI MOSFET. *IEEE Transactions on Electron Devices*, **2004**, 51, 1463-1467	2.9	100
35	Evidence for suppressed short-channel effects in deep submicron dual-material gate (DMG) partially depleted SOI MOSFETs – A two-dimensional analytical approach. *Microelectronic Engineering*, **2004**, 75, 367-374	2.5	11
34	Investigation of the novel attributes of a single-halo double gate SOI MOSFET: 2D simulation study. *Microelectronics Journal*, **2004**, 35, 761-765	1.8	39
33	Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review. *IEEE Transactions on Device and Materials Reliability*, **2004**, 4, 99-109	1.6	246
32	Surface accumulation Layer transistor (SALTran): a new bipolar transistor for enhanced current gain and reduced hot-carrier degradation. *IEEE Transactions on Device and Materials Reliability*, **2004**, 4, 509-515	1.6	20
31	A new, high-voltage 4H-SiC lateral dual sidewall Schottky (LDSS) rectifier: theoretical investigation and analysis. *IEEE Transactions on Electron Devices*, **2003**, 50, 1690-1693	2.9	4
30	2D-simulation and analysis of lateral SiC N-emitter SiGe P-base Schottky metal-collector (NPM) HBT on SOI. *Microelectronics Reliability*, **2003**, 43, 1145-1149	1.2	4
29	Lateral thin-film Schottky (LTFS) rectifier on SOI: a device with higher than plane parallel breakdown voltage. *IEEE Transactions on Electron Devices*, **2002**, 49, 181-184	2.9	5
28	A new lateral PNM Schottky collector bipolar transistor (SCBT) on SOI for nonsaturating VLSI logic design. *IEEE Transactions on Electron Devices*, **2002**, 49, 1070-1072	2.9	12
27	A new low-loss lateral trench sidewall Schottky (LTSS) rectifier on SOI with high and sharp breakdown voltage. *IEEE Transactions on Electron Devices*, **2002**, 49, 1316-1319	2.9	6
26	Elimination of bipolar induced drain breakdown and single transistor latch in submicron PD SOI MOSFET. *IEEE Transactions on Reliability*, **2002**, 51, 367-370	4.6	12
25	On the iterative schemes to obtain base doping profiles for reducing base transit time in a bipolar transistor. *IEEE Transactions on Electron Devices*, **2001**, 48, 1222-1224	2.9	9
24	A new 4H-SiC lateral merged double Schottky (LMDS) rectifier with excellent forward and reverse characteristics. *IEEE Transactions on Electron Devices*, **2001**, 48, 2695-2700	2.9	23
23	Novel lateral merged double Schottky (LMDS) rectifier: proposal and design. *IET Circuits, Devices and Systems*, **2001**, 148, 165		5

22	Study of the extended p/sup +/ dual source structure for eliminating bipolar induced breakdown in submicron SOI MOSFET's. *IEEE Transactions on Electron Devices*, **2000**, 47, 1678-1680	2.9	13
21	A simple hole scattering length model for the solution of charge transport in bipolar transistors. *IEEE Transactions on Electron Devices*, **1999**, 46, 1186-1188	2.9	
20	Novel Ge-profile design for high-speed SiGe HBTs: modelling and analysis. *IET Circuits, Devices and Systems*, **1999**, 146, 291		9
19	Profile design considerations for minimizing base transit time in SiGe HBT's. *IEEE Transactions on Electron Devices*, **1998**, 45, 1725-1731	2.9	28
18	Optimum collector width of VLSI bipolar transistors for maximum f/sub max/ at high current densities. *IEEE Transactions on Electron Devices*, **1997**, 44, 903-905	2.9	1
17	Miller's approximation in VLSI and power bipolar transistors with reach-through collectors. *IEEE Transactions on Electron Devices*, **1997**, 44, 2305-2307	2.9	1
16	Selective reactive ion etching of PECVD silicon nitride over amorphous silicon in and nitrogen containing plasma gas mixtures. *Solid-State Electronics*, **1996**, 39, 33-37	1.7	7
15	Cjc and the output conductance of advanced bipolar junction transistors under nonlocal impact ionization conditions. *Solid-State Electronics*, **1996**, 39, 1819-1821	1.7	1
14	New buried P+-grid polysilicon emitter bipolar power transistor. *Solid-State Electronics*, **1995**, 38, 1854-1856	1.7	44
13	Optimum collector EPI-thickness of advanced bipolar transistors for high speed and high current operation. *Solid-State Electronics*, **1994**, 37, 1885-1887	1.7	2
12	. *IEEE Transactions on Electron Devices*, **1994**, 41, 398-402	2.9	3
11	. *IEEE Transactions on Electron Devices*, **1994**, 41, 2471-2473	2.9	5
10	Base etched selfaligned transistor technology for advanced polyemitter bipolar transistors. *Electronics Letters*, **1994**, 30, 819-820	1.1	1
9	. *IEEE Transactions on Electron Devices*, **1993**, 40, 1478-1483	2.9	21
8	. *IEEE Transactions on Electron Devices*, **1990**, 37, 2395-2398	2.9	4
7	. *IEEE Transactions on Electron Devices*, **1989**, 36, 1803-1810	2.9	8
6	The effects of collector lifetime on the characteristics of high-voltage power transistors operating in the quasi-saturation region. *IEEE Transactions on Electron Devices*, **1987**, 34, 1163-1169	2.9	14
5	On the dominant recombination level of platinum in silicon. *Physica Status Solidi A*, **1985**, 87, 651-655		4

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