Byungsub Kim

List of Publications by Year
in descending order

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75	809	623734	552781
papers	citations	14 h-index	26 g-index

75	75	75	853
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A Compact Single-Ended Inverter-Based Transceiver With Swing Improvement for Short-Reach Links. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 3679-3688.	5.4	3
2	A DFE-Enhanced Phase-Difference Modulation Signaling for Multi-Drop Memory Interfaces. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1862-1866.	3.0	1
3	A 7.8-Gb/s 2.9-pJ/b Single-Ended Receiver With 20-Tap DFE for Highly Reflective Channels. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 818-822.	3.1	8
4	A Body Channel Communication Technique Utilizing Decision Feedback Equalization. IEEE Access, 2020, 8, 198468-198481.	4.2	6
5	A pattern-dependent injection-locked CDR for clock-embedded signaling. Microelectronics Journal, 2020, 96, 104708.	2.0	1
6	Low-Power Small-Area Inverter-Based DSM for MEMS Microphone. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2392-2396.	3.0	1
7	A 7.8 Gb/s/pin, 1.96 pJ/b Transceiver With Phase-Difference-Modulation Signaling for Highly Reflective Interconnects. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2114-2127.	5.4	5
8	An 18-Gb/s NRZ Transceiver With a Channel-Included 2-UI Impulse-Response Filtering FFE and 1-Tap DFE Compensating up to 32-dB Loss. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2863-2867.	3.0	6
9	A Multilayer-Learning Current-Mode Neuromorphic System With Analog-Error Compensation. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 986-998.	4.0	4
10	A Quadrature RC Oscillator With Noise Reduction by Voltage Swing Control. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3077-3088.	5.4	12
11	A 192-pW Voltage Reference Generating Bandgapâ€“$V_{ext{th}}$ With Process and Temperature Dependence Compensation. IEEE Journal of Solid-State Circuits, 2019, 54, 3281-3291.	5.4	46
12	A Code Inversion Encoding Technique to Improve Read Margin of A Cross-Point Phase Change Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1811-1818.	3.1	1
13	Impact of Line Mismatch on Two-Wire Deembedding Methods in Early Characterization of Emerging Interconnects. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 905-912.	2.5	0
14	A Simple Low-Cost Electric-Contact-Assisted Alignment Method for Die Stacking on an Interposer or a Printed Circuit Board. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 367-374.	2.5	0
15	Parallel Branching of Two 2-DIMM Sections With Write-Direction Impedance Matching for an 8-Drop 6.4-Gb/s SDRAM Interface. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 336-342.	2.5	4
16	Analog-digital Mixed-mode 10-tap Tomlinson-Harashima Precoding Equalizer for Single-ended High-speed Transmitter. Journal of Semiconductor Technology and Science, 2019, 19, 461-469.	0.4	0
17	A 9.3 nW all-in-one bandgap voltage and current reference circuit using leakage-based PTAT generation and DIBL characteristic. , 2018, , .		5
18	An Approximate Closed-Form Transfer Function Model for Multiconductor Transmission Lines. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1199-1203.	3.0	2

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19	An On-Chip Learning Neuromorphic Autoencoder With Current-Mode Transposable Memory Read and Virtual Lookup Table. IEEE Transactions on Biomedical Circuits and Systems, 2018, 12, 161-170.	4.0	15
20	An 84.6-dB-SNDR and 98.2-dB-SFDR Residue-Integrated SAR ADC for Low-Power Sensor Applications. IEEE Journal of Solid-State Circuits, 2018, 53, 404-417.	5.4	24
21	A low-power wide dynamic-range current readout circuit for biosensors. , 2018, , .		0
22	A 7.8Gb/s/pin 1.96pJ/b compact single-ended TRX and CDR with phase-difference modulation for highly reflective memory interfaces. , 2018, , .		10
23	An FFE Transmitter Which Automatically and Adaptively Relaxes Impedance Matching. IEEE Journal of Solid-State Circuits, 2018, 53, 1780-1792.	5.4	12
24	A 12-Gb/s AC-Coupled FFE TX With Adaptive Relaxed Impedance Matching Achieving Adaptation Range of 35-75Î© Z<inf>0</inf> and 30-550Î© R<inf>RX</inf>. , 2018, , .		0
25	A Rule-of-thumb Condition to Avoid Large HRS Current in ReRAM Crossbar Array Design. , 2018, , .		1
26	A Search Algorithm for the Worst Operation Scenario of a Cross-Point Phase-Change Memory Utilizing Particle Swarm Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2591-2598.	3.1	3
27	A Study on Bandgap Reference Circuit With Leakage-Based PTAT Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2310-2321.	3.1	11
28	Design of Digital CMOS Neuromorphic IC with Current-starved SRAM Synapse for Unsupervised Stochastic Learning. Journal of Semiconductor Technology and Science, 2018, 18, 65-77.	0.4	2
29	A 250- $muext{W}$ 2.4-GHz Fast-Lock Fractional-N Frequency Generation for Ultralow-Power Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 106-110.	3.0	7
30	An Approximate Transfer Function Model of Two Serially Connected Heterogeneous Transmission Lines. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1067-1071.	3.0	2
31	Automatic ReRAM SPICE Model Generation From Empirical Data for Fast ReRAM-Circuit Coevaluation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1821-1830.	3.1	6
32	5.5 A quadrature relaxation oscillator with a process-induced frequency-error compensation loop. , 2017, , .		24
33	A Low-Power Wide Dynamic-Range Current Readout Circuit for Ion-Sensitive FET Sensors. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 523-533.	4.0	23
34	A Self-Biased Current-Mode Amplifier With an Application to 10-bit Pipeline ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1706-1717.	5.4	7
35	Investigation on the Worst Read Scenario of a ReRAM Crossbar Array. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2402-2410.	3.1	6
36	All-Synthesizable Current-Mode Transmitter Driver for USB2.0 Interface. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 788-792.	3.1	4

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37	A 10-GHz multi-purpose reconfigurable built-in self-test circuit for high-speed links. , 2017, , .		5
38	An FFE TX with 3.8x eye improvement by automatic impedance adaptation for universal compatibility with arbitrary channel and RX impedances. , 2017, , .		7
39	All-synthesizable 6Gbps voltage-mode transmitter for serial link. , 2016, , .		0
40	Read margin analysis in an ReRAM crossbar array. , 2016, , .		1
41	An ECG monitoring system using android smart phone. , 2016, , .		3
42	A low-power LDO circuit with a fast load regulation. , 2016, , .		3
43	A Reconfigurable and Portable Highly Sensitive Biosensor Platform for ISFET and Enzyme-Based Sensors. IEEE Sensors Journal, 2016, 16, 4443-4451.	4.7	11
44	A SNR-Enhanced Mutual-Capacitive Touch-Sensor ROIC Using an Averaging With Three Specific TX Frequencies, a Noise Memory, and a Compact Delay Compensation Circuit. IEEE Sensors Journal, 2016, 16, 6931-6938.	4.7	12
45	A Single-Ended Parallel Transceiver With Four-Bit Four-Wire Four-Level Balanced Coding for the Point-to-Point DRAM Interface. IEEE Journal of Solid-State Circuits, 2016, 51, 1890-1901.	5.4	11
46	A Coefficient-Error-Robust Feed-Forward Equalizing Transmitter for Eye-Variation and Power Improvement. IEEE Journal of Solid-State Circuits, 2016, 51, 1902-1914.	5.4	5
47	A 0.65-to-10.5 Gb/s Reference-Less CDR With Asynchronous Baud-Rate Sampling for Frequency Acquisition and Adaptive Equalization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 276-287.	5.4	19
48	An approximate condition to avoid reverse leakage current in ReRAM crossbar design. , 2015, , .		6
49	A reduced-size look-up-table for ADC sample-times of a single-chip non-uniform-sampling digital-beamformer for ultrasound medical imaging. , 2015, , .		1
50	A sample reduction technique by aliasing channel response for fast equalizing transceiver design. , 2015, , .		4
51	A threshold voltage variation calibration algorithm for an ISFET-based low-cost pH sensor system. , 2015, , .		0
52	An FPGA-based embedded system for portable and cost-efficient bio-sensing: A low-cost controller for biomedical diagnosis. , 2015, , .		0
53	An LCD-VCOM-Noise Resilient Mutual-Capacitive Touch-Sensor IC Chip With a Low-Voltage Driving Signal. IEEE Sensors Journal, 2015, 15, 4595-4602.	4.7	22
54	An Approximate Closed-Form Transfer Function Model for Diverse Differential Interconnects. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1335-1344.	5.4	12

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55	An input pole tuned switching equalization scheme for high-speed serial links. , 2015, , .		0
56	Analytical Formulas for Tradeoff Among Channel Loss, Length, and Frequency of <inline-formula> <tex-math notation="LaTeX">RC </tex-math></inline-formula>- and <inline-formula> <tex-math notation="LaTeX">LC </tex-math></inline-formula>-Dominant Single-Ended Interconnects for Fast Equalized Link Tradeoff Estimation. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2015, 5, 1497-1506.	2.5	3
57	An Analog-Digital Hybrid RX Beamformer Chip With Non-Uniform Sampling for Ultrasound Medical Imaging With 2D CMUT Array. IEEE Transactions on Biomedical Circuits and Systems, 2014, 8, 799-809.	4.0	28
58	A 40-mV-Swing Single-Ended Transceiver for TSV with a Switched-Diode RX Termination. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 987-991.	3.0	6
59	An open-loop differential time amplifier. , 2014, , .		0
60	2.7 A coefficient-error-robust FFE TX with 230% eye-variation improvement without calibration in 65nm CMOS technology. , 2014, , .		3
61	Analysis of an Open-Loop Time Amplifier With a Time Gain Determined by the Ratio of Bias Current. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 481-485.	3.0	21
62	An 80 mV-Swing Single-Ended Duobinary Transceiver With a TIA RX Termination for the Point-to-Point DRAM Interface. IEEE Journal of Solid-State Circuits, 2014, 49, 2618-2630.	5.4	24
63	An Approximate Closed-Form Channel Model for Diverse Interconnect Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 3034-3043.	5.4	11
64	A 0.5-V, 1.47- $muhbox{W}$ 40-kS/s 13-bit SAR ADC With Capacitor Error Compensation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 840-844.	3.0	14
65	Current-Mode Transceiver for Silicon Interposer Channel. IEEE Journal of Solid-State Circuits, 2014, 49, 2044-2053.	5.4	27
66	A 5 Gb/s Single-Ended Parallel Receiver With Adaptive Crosstalk-Induced Jitter Cancellation. IEEE Journal of Solid-State Circuits, 2013, 48, 2118-2127.	5.4	13
67	A 10-bit 25-MS/s 1.25-mW Pipelined ADC With a Semidigital Gm-Based Amplifier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 142-146.	3.0	6
68	A FIR-Embedded Phase Interpolator Based Noise Filtering for Wide-Bandwidth Fractional-N PLL. IEEE Journal of Solid-State Circuits, 2013, 48, 2795-2804.	5.4	31
69	A QDR-Based 6-GB/s Parallel Transceiver With Current-Regulated Voltage-Mode Output Driver and Byte CDR for Memory Interface. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 91-95.	3.0	4
70	A 1.9-GHz Fractional-N Digital PLL With Subexponent $ DeltaSigma$ TDC and IIR-Based Noise Cancellation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 721-725.	3.0	3
71	An Energy-Efficient Equalized Transceiver for RC-Dominant Channels. IEEE Journal of Solid-State Circuits, 2010, 45, 1186-1197.	5.4	43
72	A 10-Gb/s Compact Low-Power Serial I/O With DFE-IIR Equalization in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2009, 44, 3526-3538.	5.4	163

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73	Characterization of Equalized and Repeated Interconnects for NoC Applications. IEEE Design and Test of Computers, 2008, 25, 430-439.	1.0	21
74	Equalized interconnects for on-chip networks: modeling and optimization framework. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	2
75	Power-adaptive operational amplifier with positive-feedback self biasing. , 0, , .		2