Siamak Mohammadi

List of Publications by Year in Descending Order

73 papers	416 citations	11 h-index	16 g-index
97 ext. papers	552 ext. citations	2.3 avg, IF	4.06 L-index

#	Paper	IF	Citations
73	Towards Efficient Logic-in-Memory Computing with Magnetic Reconfigurable Logic Circuits. *IEEE Magnetics Letters*, **2022**, 1-1	1.6	1
72	THAMON: Thermal-aware High-performance Application Mapping onto Opto-electrical network-on-chip. *Journal of Systems Architecture*, **2021**, 102315	5.5	1
71	ICES: an innovative crosstalk-efficient 2 □2 photonic-crystal switch. *Optical and Quantum Electronics* , **2021**, 53, 1	2.4	2
70	Low-power and variation-aware approximate arithmetic units for Image Processing Applications. *AEU - International Journal of Electronics and Communications*, **2021**, 138, 153825	2.8	1
69	Prediction-based underutilized and destination host selection approaches for energy-efficient dynamic VM consolidation in data centers. *Journal of Supercomputing*, **2020**, 76, 10240-10257	2.5	10
68	Vulnerability assessment of fault-tolerant optical network-on-chips. *Journal of Parallel and Distributed Computing*, **2020**, 145, 140-159	4.4	7
67	Infrastructure Aware Heterogeneous-Workloads Scheduling for Data Center Energy Cost Minimization. *IEEE Transactions on Cloud Computing*, **2020**, 1-1	3.3	1
66	Insertion loss-aware application mapping onto the optical Cube-Connected Cycles architecture. *Computers and Electrical Engineering*, **2020**, 82, 106559	4.3	9
65	Power loss analysis in thermally-tuned nanophotonic switch for on-chip interconnect. *Nano Communication Networks*, **2020**, 26, 100323	2.9	5
64	Process variation-aware approximate full adders for imprecision-tolerant applications. *Computers and Electrical Engineering*, **2020**, 87, 106761	4.3	3
63	SORT. *ACM Transactions on Modeling and Performance Evaluation of Computing Systems*, **2019**, 4, 1-25	0.8	3
62	MAGNETIC: Multi-Agent Machine Learning-Based Approach for Energy Efficient Dynamic Consolidation in Data Centers. *IEEE Transactions on Services Computing*, **2019**, 1-1	4.8	9
61	A Variation-Aware Ternary Spin-Hall Assisted STT-RAM Based on Hybrid MTJ/GAA-CNTFET Logic. *IEEE Nanotechnology Magazine*, **2019**, 18, 598-605	2.6	31
60	CMV: Clustered Majority Voting Reliability-Aware Task Scheduling for Multicore Real-Time Systems. *IEEE Transactions on Reliability*, **2019**, 68, 187-200	4.6	4
59	Exploration of approximate multipliers design space using carry propagation free compressors **2018**,		1
58	A Majority-Based Reliability-Aware Task Mapping in High-Performance Homogenous NoC Architectures. *Transactions on Embedded Computing Systems*, **2018**, 17, 1-31	1.8	6
57	Elastic buffer evaluation for link pipelining under process variation. *IET Circuits, Devices and Systems* , **2018**, 12, 645-654	1.1	3

56	A high performance dual clock elastic FIFO network interface for GALS NoC. *Microelectronics Journal*, **2018**, 76, 69-80	1.8	1
55	Energy efficient configuration unification and compression for CGRAs. *Microprocessors and Microsystems*, **2018**, 62, 1-11	2.4	0
54	LORAP: Low-Overhead Power and Reliability-Aware Task Mapping Based on Instruction Footprint for Real-Time Applications **2017**,		3
53	A self-organized load balancing mechanism for cloud computing. *Concurrency Computation Practice and Experience*, **2017**, 29, e3897	1.4	1
52	CAL: Exploring cost, accuracy, and latency in approximate and speculative adder design **2017**,		2
51	A Majority-Based Reliability-Aware Task-Mapping in High-Performance Homogenous NoC Architectures **2016**,		1
50	Reliability-Aware Task Scheduling using Clustered Replication for Multi-core Real-Time systems **2016**,		6
49	Statistical analysis of asynchronous pipelines in presence of process variation using formal models. *The Integration VLSI Journal*, **2016**, 55, 98-117	1.4	1
48	Gem5v: a modified gem5 for simulating virtualized systems. *Journal of Supercomputing*, **2015**, 71, 1484-1504	2.5	5
47	Hypervisor and Neighbors Noise: Performance Degradation in Virtualized Environments. *IEEE Transactions on Services Computing*, **2015**, 1-1	4.8	4
46	Architecture Support for Tightly-Coupled Multi-Core Clusters with Shared-Memory HW Accelerators. *IEEE Transactions on Computers*, **2015**, 64, 2132-2144	2.5	8
45	Distributed consolidation of virtual machines for power efficiency in heterogeneous cloud data centers. *Computers and Electrical Engineering*, **2015**, 47, 173-185	4.3	16
44	Variation-aware approaches with power improvement in digital circuits. *The Integration VLSI Journal*, **2015**, 48, 83-100	1.4	7
43	A Low-Overhead, Fully-Distributed, Guaranteed-Delivery Routing Algorithm for Faulty Network-on-Chips **2015**,		11
42	Demystifying SWCNT-bundle-interconnects inductive behavior through novel modeling. *Journal of Computational Electronics*, **2013**, 12, 1-13	1.8	1
41	Distributed fair DRAM scheduling in network-on-chips architecture. *Journal of Systems Architecture*, **2013**, 59, 543-550	5.5	1
40	Quota setting router architecture for quality of service in GALS NoC **2013**,		3
39	Modeling symmetrical independent gate FinFET using predictive technology model **2013**,		3

38	A platform for multi reconfigurable instruction set processor system on chip (MRPSoC) **2013**,		1
37	A synthesis algorithm for customized heterogeneous multi-processors **2012**,		1
36	Power-aware game for cloud computing: A distributed mechanism based on Game Theory for minmizing power consumption in cloud scale datacenter **2012**,		1
35	Evaluating location of memory controller in on-chip communication networks **2012**,		1
34	A tightly-coupled multi-core cluster with shared-memory HW accelerators **2012**,		10
33	Adaptive Input-Output Selection Based On-Chip Router Architecture. *Journal of Low Power Electronics*, **2012**, 8, 11-29	1.2	19
32	Mutant Fault Injection in Functional Properties of a Model to Improve Coverage Metrics **2011**,		1
31	Designing robust threshold gates against soft errors. *Microelectronics Journal*, **2011**, 42, 1276-1289	1.8	3
30	A reconfigurable and adaptive routing method for fault-tolerant mesh-based networks-on-chip. *AEU - International Journal of Electronics and Communications*, **2011**, 65, 630-640	2.8	31
29	An adaptive fuzzy logic-based routing algorithm for networks-on-chip **2011**,		16
28	Designing Robust Asynchronous Circuits Based on FinFET Technology **2011**,		2
27	Modified bundled-data as a new protocol for NoC asynchronous links. *Microelectronics Journal*, **2011**, 42, 638-647	1.8	
26	Low-energy GALS NoC with FIFO Monitoring dynamic voltage scaling. *Microelectronics Journal*, **2011**, 42, 889-896	1.8	13
25	Fault-aware and Reconfigurable Routing Algorithms for Networks-on-Chip. *IETE Journal of Research* , **2011**, 57, 215	0.9	6
24	**2010**,		1
23	Dynamic voltage scaling for fully asynchronous NoCs using FIFO threshold levels **2010**,		2
22	History-Based Dynamic Voltage Scaling with Few Number of Voltage Modes for GALS NoC **2010**,		3
21	A High Throughput Low Power FIFO Used for GALS NoC Buffers **2010**,		12

20	A fault-tolerant and congestion-aware routing algorithm for Networks-on-Chip **2010**,		17
19	A fault-aware, reconfigurable and adaptive routing algorithm for NoC applications **2010**,		4
18	A dual mode UHF EPC Gen 2 RFID tag in 0.18μm CMOS. *Microelectronics Journal*, **2010**, 41, 458-464	1.8	8
17	An efficent dynamic multicast routing protocol for distributing traffic in NOCs **2009**,		12
16	Low-cost fault tolerance in evolvable multiprocessor systems: a graceful degradation approach. *Journal of Zhejiang University: Science A*, **2009**, 10, 922-926	2.1	1
15	Reliability assessment of networks-on-chip based on analytical models. *Journal of Zhejiang University: Science A*, **2009**, 10, 1801-1814	2.1	3
14	Comparison of dual rail and an enhanced bundled data asynchronous protocols noise robustness in the GALS NoC link application **2009**,		1
13	A Hazard-Free Delay-Insensitive 4-phase On-Chip Link Using MVCM Signaling **2009**,		1
12	Low-distance path-based multicast routing algorithm for network-on-chips. *IET Computers and Digital Techniques*, **2009**, 3, 430	0.9	29
11	A dual mode EPC Gen 2 UHF RFID transponder in 0.18μm CMOS **2008**,		3
10	Efficient clustering of wireless sensor networks based on memetic algorithm **2008**,		4
9	PAMPR: Power-aware and minimum path routing algorithm for NoCs **2008**,		6
8	A low power baseband processor for a dual mode UHF EPC Gen 2 RFID tag **2008**,		9
7	Designing an MPSoC architecture with run-time and evolvable task decomposition and scheduling: A neural network case study **2008**,		1
6	An energy efficient routing protocol for cluster-based wireless sensor networks using ant colony optimization **2008**,		16
5	Enhancing the Testability of RTL Designs Using Efficiently Synthesized Assertions **2008**,		3
4	Graph based test case generation for TLM functional verification. *Microprocessors and Microsystems*, **2008**, 32, 288-295	2.4	1
3	Functional Test-Case Generation by a Control Transaction Graph for TLM Verification **2007**,		1

2 Assignment coverage, a complementary coverage metric in formal verification **2007**, 1

1 Improved Assertion Lifetime via Assertion-Based Testing Methodology **2006**, 1