Siamak Mohammadi

List of Publications by Year
in descending order

96	677	840119 11	794141 19
papers	citations	h-index	g-index

97	97	97	464
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A Variation-Aware Ternary Spin-Hall Assisted STT-RAM Based on Hybrid MTJ/GAA-CNTFET Logic. IEEE Nanotechnology Magazine, 2019, 18, 598-605.	1.1	47
2	A reconfigurable and adaptive routing method for fault-tolerant mesh-based networks-on-chip. AEU - International Journal of Electronics and Communications, 2011, 65, 630-640.	1.7	42
3	Low-distance path-based multicast routing algorithm for network-on-chips. IET Computers and Digital Techniques, 2009, 3, 430.	0.9	40
4	Adaptive Input-Output Selection Based On-Chip Router Architecture. Journal of Low Power Electronics, 2012, 8, 11-29.	0.6	25
5	A fault-tolerant and congestion-aware routing algorithm for Networks-on-Chip. , 2010, , .		23
6	An adaptive fuzzy logic-based routing algorithm for networks-on-chip. , 2011, , .		23
7	MAGNETIC: Multi-Agent Machine Learning-Based Approach for Energy Efficient Dynamic Consolidation in Data Centers. IEEE Transactions on Services Computing, 2022, 15, 30-44.	3.2	23
8	Distributed consolidation of virtual machines for power efficiency in heterogeneous cloud data centers. Computers and Electrical Engineering, 2015, 47, 173-185.	3.0	21
9	Prediction-based underutilized and destination host selection approaches for energy-efficient dynamic VM consolidation in data centers. Journal of Supercomputing, 2020, 76, 10240-10257.	2.4	21
10	An energy efficient routing protocol for cluster-based wireless sensor networks using ant colony optimization. , 2008, , .		20
11	Process variation-aware approximate full adders for imprecision-tolerant applications. Computers and Electrical Engineering, 2020, 87, 106761.	3.0	19
12	An efficent dynamic multicast routing protocol for distributing traffic in NOCs. , 2009, , .		18
13	A Low-Overhead, Fully-Distributed, Guaranteed-Delivery Routing Algorithm for Faulty Network-on-Chips. , 2015, , .		17
14	A High Throughput Low Power FIFO Used for GALS NoC Buffers. , 2010, , .		16
15	A low power baseband processor for a dual mode UHF EPC Gen 2 RFID tag. , 2008, , .		15
16	Low-energy GALS NoC with FIFOâ€"Monitoring dynamic voltage scaling. Microelectronics Journal, 2011, 42, 889-896.	1.1	15
17	Insertion loss-aware application mapping onto the optical Cube-Connected Cycles architecture. Computers and Electrical Engineering, 2020, 82, 106559.	3.0	14
18	Low-power and variation-aware approximate arithmetic units for Image Processing Applications. AEU - International Journal of Electronics and Communications, 2021, 138, 153825.	1.7	13

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19	Architecture Support for Tightly-Coupled Multi-Core Clusters with Shared-Memory HW Accelerators. IEEE Transactions on Computers, 2015, 64, 2132-2144.	2.4	12
20	A dual mode UHF EPC Gen 2 RFID tag in 0.18Î¼m CMOS. Microelectronics Journal, 2010, 41, 458-464.	1.1	11
21	A tightly-coupled multi-core cluster with shared-memory HW accelerators. , 2012, , .		11
22	Vulnerability assessment of fault-tolerant optical network-on-chips. Journal of Parallel and Distributed Computing, 2020, 145, 140-159.	2.7	11
23	Infrastructure Aware Heterogeneous-Workloads Scheduling for Data Center Energy Cost Minimization. IEEE Transactions on Cloud Computing, 2022, 10, 972-983.	3.1	11
24	Fault-aware and Reconfigurable Routing Algorithms for Networks-on-Chip. IETE Journal of Research, 2011, 57, 215.	1.8	10
25	Power loss analysis in thermally-tuned nanophotonic switch for on-chip interconnect. Nano Communication Networks, 2020, 26, 100323.	1.6	10
26	Reliability-Aware Task Scheduling using Clustered Replication for Multi-core Real-Time systems. , 2016, , .		9
27	PAMPR: Power-aware and minimum path routing algorithm for NoCs. , 2008, , .		8
28	Gem5v: a modified gem5 for simulating virtualized systems. Journal of Supercomputing, 2015, 71, 1484-1504.	2.4	8
29	Variation-aware approaches with power improvement in digital circuits. The Integration VLSI Journal, 2015, 48, 83-100.	1.3	8
30	Enhancing the Testability of RTL Designs Using Efficiently Synthesized Assertions. , 2008, , .		7
31	A Majority-Based Reliability-Aware Task Mapping in High-Performance Homogenous NoC Architectures. Transactions on Embedded Computing Systems, 2018, 17, 1-31.	2.1	7
32	CMV: Clustered Majority Voting Reliability-Aware Task Scheduling for Multicore Real-Time Systems. IEEE Transactions on Reliability, 2019, 68, 187-200.	3.5	7
33	History-Based Dynamic Voltage Scaling with Few Number of Voltage Modes for GALS NoC. , 2010, , .		6
34	A fault-aware, reconfigurable and adaptive routing algorithm for NoC applications. , 2010, , .		6
35	Efficient clustering of wireless sensor networks based on memetic algorithm. , 2008, , .		5
36	Designing robust threshold gates against soft errors. Microelectronics Journal, 2011, 42, 1276-1289.	1.1	5

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37	Quota setting router architecture for quality of service in GALS NoC. , 2013, , .		5
38	Modeling symmetrical independent gate FinFET using predictive technology model. , 2013, , .		5
39	Hypervisor and Neighborsâ€™ Noise: Performance Degradation in Virtualized Environments. IEEE Transactions on Services Computing, 2015, , 1-1.	3.2	5
40	SORT. ACM Transactions on Modeling and Performance Evaluation of Computing Systems, 2019, 4, 1-25.	0.8	5
41	ICES: an innovative crosstalk-efficient 2ÂÃ—Â2 photonic-crystal switch. Optical and Quantum Electronics, 2021, 53, 1.	1.5	5
42	THAMON: Thermal-aware High-performance Application Mapping onto Opto-electrical network-on-chip. Journal of Systems Architecture, 2021, 121, 102315.	2.5	5
43	Toward Efficient Logic-in-Memory Computing With Magnetic Reconfigurable Logic Circuits. IEEE Magnetics Letters, 2022, 13, 1-5.	0.6	5
44	A dual mode EPC Gen 2 UHF RFID transponder in 0.18μm CMOS. , 2008, , .		4
45	Designing Robust Asynchronous Circuits Based on FinFET Technology. , 2011, , .		4
46	Exploration of approximate multipliers design space using carry propagation free compressors. , 2018, , .		4
47	Elastic buffer evaluation for link pipelining under process variation. IET Circuits, Devices and Systems, 2018, 12, 645-654.	0.9	4
48	Reliability assessment of networks-on-chip based on analytical models. Journal of Zhejiang University: Science A, 2009, 10, 1801-1814.	1.3	3
49	Dynamic voltage scaling for fully asynchronous NoCs using FIFO threshold levels. , 2010, , .		3
50	A selfâ€organized load balancing mechanism for cloud computing. Concurrency Computation Practice and Experience, 2017, 29, e3897.	1.4	3
51	CAL: Exploring cost, accuracy, and latency in approximate and speculative adder design. , 2017, , .		3
52	LORAP: Low-Overhead Power and Reliability-Aware Task Mapping Based on Instruction Footprint for Real-Time Applications. , 2017, , .		3
53	A high performance dual clock elastic FIFO network interface for GALS NoC. Microelectronics Journal, 2018, 76, 69-80.	1.1	3
54	Improved Assertion Lifetime via Assertion-Based Testing Methodology. , 2006, , .		2

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55	Functional Test-Case Generation by a Control Transaction Graph for TLM Verification. , 2007, , .		2
56	Graph based test case generation for TLM functional verification. Microprocessors and Microsystems, 2008, 32, 288-295.	1.8	2
57	Designing an MPSoC architecture with run-time and evolvable task decomposition and scheduling: A neural network case study. , 2008, , .		2
58	Comparison of dual rail and an enhanced bundled data asynchronous protocols noise robustness in the GALS NoC link application. , 2009, , .		2
59	A high-throughput, metastability-free GALS channel based on pausible clock method. , 2010, , .		2
60	A synthesis algorithm for customized heterogeneous multi-processors. , 2012, , .		2
61	Power-aware game for cloud computing: A distributed mechanism based on Game Theory for minmizing power consumption in cloud scale datacenter. , 2012, , .		2
62	Demystifying SWCNT-bundle-interconnects inductive behavior through novel modeling. Journal of Computational Electronics, 2013, 12, 1-13.	1.3	2
63	A platform for multi reconfigurable instruction set processor system on chip (MRPSoC). , 2013, , .		2
64	Statistical analysis of asynchronous pipelines in presence of process variation using formal models. The Integration VLSI Journal, 2016, 55, 98-117.	1.3	2
65	A Majority-Based Reliability-Aware Task-Mapping in High-Performance Homogenous NoC Architectures. , 2016, , .		2
66	LRTM: Life-time and Reliability-aware Task Mapping Approach for Heterogeneous Multi-core Systems. , 2018, , .		2
67	Energy efficient configuration unification and compression for CGRAs. Microprocessors and Microsystems, 2018, 62, 1-11.	1.8	2
68	A Magnetic Reconfigurable Ternary NOR/NAND Logic for Logic-in-Memory Applications. Spin, 0, , .	0.6	2
69	HDMS: high-performance dual-shaped microring-resonator-based optical switch. Optical Engineering, 2022, 61, .	0.5	2
70	Assignment coverage, a complementary coverage metric in formal verification. , 2007, , .		1
71	Input Stimuli Evolution for RFID Tag Functional Verification. , 2007, , .		1
72	Architectural Synthesis with Control Data Flow Extraction toward an Asynchronous CAD Tool. , 2008, , .		1

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73	An Efficient Fault Simulator for QDI Asynchronous Circuits. , 2008, , .		1
74	Inherent reliability evaluation of Networks-on-Chip based on analytical models. , 2008, , .		1
75	Exhaustive Data Path Optimization in High-Level Synthesis through Area Improvement. , 2009, , .		1
76	Low-cost fault tolerance in evolvable multiprocessor systems: a graceful degradation approach. Journal of Zhejiang University: Science A, 2009, 10, 922-926.	1.3	1
77	A Hazard-Free Delay-Insensitive 4-phase On-Chip Link Using MVCM Signaling. , 2009, , .		1
78	Mutant Fault Injection in Functional Properties of a Model to Improve Coverage Metrics. , 2011, , .		1
79	Evaluating location of memory controller in on-chip communication networks. , 2012, , .		1
80	Distributed fair DRAM scheduling in network-on-chips architecture. Journal of Systems Architecture, 2013, 59, 543-550.	2.5	1
81	Clustering Effects on the Design of Opto-Electrical Network-on-Chip. , 2016, , .		1
82	A New Fair Dynamic Routing Algorithm for Avoiding Hot Spots in NoCs. , 2006, , .		0
83	A Superior Low Complexity Rate Control Algorithm. , 2007, , .		0
84	A novel test environment for template based QDI asynchronous circuits. , 2008, , .		0
85	A novel relational model based hardware simulator. , 2008, , .		0
86	Particle Swarm Optimization for Run-Time Task Decomposition and Scheduling in Evolvable MPSoC. , 2009, , .		0
87	Data path refinement algorithm in high-level synthesis based on dynamic programming. , 2009, , .		0
88	Universal on-chip communication channel. , 2010, , .		0
89	On the Potentials of FinFETs for Asynchronous Circuit Design. , 2011, , .		0
90	Fast and accurate SWCNT bundle magnetic inductance models. , 2011, , .		0

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91	Modified bundled-data as a new protocol for NoC asynchronous links. Microelectronics Journal, 2011, 42, 638-647.	1.1	0
92	Power and Variability Improvement of an Asynchronous Router Using Stacking and Dual-Vth Approaches. , 2013, , .		0
93	High-Speed, Low-Power Quasi Delay Insensitive Handshake Circuits Based on FinFET Technology. , 2014, , .		0
94	Cache Energy Management through Dynamic Reconfiguration Approach in Opto-Electrical NoC. , 2017, , .		0
95	Optimized Assignment Coverage Computation in Formal Verification of Digital Systems. Proceedings of the Asian Test Symposium, 2007, , .	0.0	0
96	High-level Modeling and Verification Platform for Elastic Circuits with Process Variation Considerations. ACM Journal on Emerging Technologies in Computing Systems, 0, , .	1.8	0