Otmane Ait-Mohamed

List of Publications by Year
in descending order

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96	581	840776 11	839539 18
papers	citations	h-index	g-index

99	99	99	382
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Routing and Scheduling of Time-Triggered Traffic in Time-Sensitive Networks. IEEE Transactions on Industrial Informatics, 2020, 16, 4525-4534.	11.3	82
2	A formal verification framework for SysML activity diagrams. Expert Systems With Applications, 2014, 41, 2713-2728.	7.6	32
3	Fault-Resilient Topology Planning and Traffic Configuration for IEEE 802.1Qbv TSN Networks. , 2018, , .		26
4	A Survey on Computer-Aided Diagnosis of Brain Disorders through MRI Based on Machine Learning and Data Mining Methodologies with an Emphasis on Alzheimer Disease Diagnosis and the Contribution of the Multimodal Fusion. Applied Sciences (Switzerland), 2020, 10, 1894.	2.5	24
5	Computer-Aided Diagnosis System of Alzheimer's Disease Based on Multimodal Fusion: Tissue Quantification Based on the Hybrid Fuzzy-Genetic-Possibilistic Model and Discriminative Classification Based on the SVDD Model. Brain Sciences, 2019, 9, 289.	2.3	21
6	Model Checking for a First-Order Temporal Logic Using Multiway Decision Graphs (MDGs). Computer Journal, 2004, 47, 71-84.	2.4	19
7	Characterizing, modeling, and analyzing soft error propagation in asynchronous and synchronous digital circuits. Microelectronics Reliability, 2015, 55, 238-250.	1.7	17
8	New Insights Into the Single Event Transient Propagation Through Static and TSPC Logic. IEEE Transactions on Nuclear Science, 2014, 61, 1618-1627.	2.0	15
9	A Security Risk Assessment Framework for SysML Activity Diagrams. , 2013, , .		13
10	Formal analysis of SEU mitigation for early dependability and performability analysis of FPGA-based space applications. Journal of Applied Logic, 2017, 25, 47-68.	1.1	13
11	A hybrid camera- and ultrasound-based approach for needle localization and tracking using a 3D motorized curvilinear ultrasound probe. Medical Image Analysis, 2018, 50, 145-166.	11.6	13
12	Towards an Accurate Probabilistic Modeling and Statistical Analysis of Temporal Faults via Temporal Dynamic Fault-Trees (TDFTs). IEEE Access, 2019, 7, 29264-29276.	4.2	12
13	Dependability modeling and optimization of triple modular redundancy partitioning for SRAM-based FPGAs. Reliability Engineering and System Safety, 2019, 182, 107-119.	8.9	12
14	Safety analysis of train control system based on model-driven design methodology. Computers in Industry, 2019, 105, 1-16.	9.9	12
15	Towards Safe and Robust Closed-Loop Artificial Pancreas Using Improved PID-Based Control Strategies. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3147-3157.	5.4	12
16	Integrating SAT with Multiway Decision Graphs for efficient model checking. , 2007, , .		11
17	A Comparative Study of Parallel Prefix Adders in FPGA Implementation of EAC. , 2009, , .		10
18	Model-based systems security quantification. , 2011, , .		10

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19	A quantitative verification framework of SysML activity diagrams under time constraints. Expert Systems With Applications, 2015, 42, 7493-7510.	7.6	10
20	Reliability-driven Automotive Software Deployment based on a Parametrizable Probabilistic Model Checking. Expert Systems With Applications, 2021, 174, 114572.	7.6	10
21	Modeling, analyzing, and abstracting single event transient propagation at gate level. , 2014, , .		9
22	A property-based abstraction framework for SysML activity diagrams. Knowledge-Based Systems, 2014, 56, 328-343.	7.1	9
23	A probabilistic and timed verification approach of SysML state machine diagram. , 2015, , .		9
24	A probabilistic verification framework of SysML activity diagrams. , 2013, , .		8
25	Reachability analysis using multiway decision graphs in the HOL theorem prover. , 2008, , .		7
26	High Level Reduction Technique for Multiway Decision Graphs Based Model Checking. , 0, , .		7
27	Verification of the Correctness in Composed UML Behavioural Diagrams. Studies in Computational Intelligence, 2010, , 163-177.	0.9	6
28	Towards An Accurate Reliability, Availability and Maintainability Analysis Approach for Satellite Systems Based on Probabilistic Model Checking. , 2015, , .		6
29	Efficient and accurate analysis of single event transients propagation using SMT-based techniques. , 2016, , .		6
30	Efficient probabilistic fault tree analysis of safety critical systems via probabilistic model checking. , 2016, , .		6
31	Formal analysis of fault tree using probabilistic model checking: A solar array case study. , 2016, , .		6
32	System-Level Analysis of the Vulnerability of Processors Exposed to Single-Event Upsets via Probabilistic Model Checking. IEEE Transactions on Nuclear Science, 2017, 64, 2523-2530.	2.0	6
33	FPGA Implementation and Performance Evaluation of a Digital Carrier Synchronizer Using Different Numerically Controlled Oscillators. , 2007, , .		5
34	An Abstract Reachability Approach by Combining HOL Induction and Multiway Decision Graphs. Journal of Computer Science and Technology, 2009, 24, 76-95.	1.5	5
35	A re-usable verification framework of Open Core Protocol (OCP). , 2009, , .		5
36	Symmetry Reduction of Time-Triggered Ethernet Protocol. Procedia Computer Science, 2013, 19, 273-280.	2.0	5

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37	Efficient multilevel formal analysis and estimation of design vulnerability to Single Event Transients. , 2015, , .		5
38	Computer-Aided Diagnosis System for Alzheimer's Disease Using Fuzzy-Possibilistic Tissue Segmentation and SVM Classification. , 2018, , .		5
39	Towards System Level Security Analysis of Artificial Pancreas Via UPPAAL-SMC. , 2019, , .		5
40	Investigating the impact of propagation paths and re-convergent paths on the propagation induced pulse broadening. , 2013, , .		4
41	Automotive safety verification under temporal failure of adaptive cruise control system using statistical model checking. , 2017, , .		4
42	MDG-BASED STATE ENUMERATION BY RETIMING AND CIRCUIT TRANSFORMATION. Journal of Circuits, Systems and Computers, 2004, 13, 1111-1132.	1.5	3
43	A New 10 Gbps Traffic Management algorithm for High-speed Networks. , 2007, , .		3
44	A case study on system-level modeling by aspect-oriented programming. , 2009, , .		3
45	NuMDG: A New Tool for Multiway Decision Graphs Construction. Journal of Computer Science and Technology, 2011, 26, 139-152.	1.5	3
46	MDG-SAT: an automated methodology for efficient safety checking. International Journal of Critical Computer-Based Systems, 2012, 3, 4.	0.1	3
47	Identification of soft error glitch-propagation paths: Leveraging SAT solvers. , 2012, , .		3
48	Abstracting Single Event Transient characteristics variations due to input patterns and fan-out. , 2014, , .		3
49	Comprehensive vulnerability analysis of systems exposed to SEUs via probabilistic model checking. , 2016, , .		3
50	Reliability Analysis of TSN Networks Under SEU Induced Soft Error Using Model Checking. , 2019, , .		3
51	Towards Safe and Robust Closed-Loop Artificial Pancreas Using Adaptive Weighted PID Control Strategy. , 2020, , .		3
52	First-Order LTL Model Checking Using MDGs. Lecture Notes in Computer Science, 2004, , 441-455.	1.3	3
53	MDG-Based Verification of the Look-Aside Interface. , 2006, , .		2
54	Analysis and Performance Evaluation of a Digital Carrier Synchronizer for Modem Applications. , 2007, , .		2

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55	The performance of combining multiway decision graphs and HOL theorem prover. , 2008, , .		2
56	SEGP-Finder: Tool for identification of Soft Error Glitch-Propagating paths at gate level. , 2011, , .		2
57	Towards an FPGA implementation and performance evaluation of a digital carrier synchronizer with a portable emulation environment. International Journal of Computer Applications in Technology, 2012, 45, 66.	0.5	2
58	Formal proof of integer adders using all-prefix-sums operation. Science China Information Sciences, 2012, 55, 1949-1960.	4.3	2
59	A Formal Approach for Maintainability and Availability Assessment Using Probabilistic Model Checking. Lecture Notes in Networks and Systems, 2016, , 295-309.	0.7	2
60	HMM/MLP speech recognition system using a novel data clustering approach. , 2017, , .		2
61	New Insights Into Soft-Faults Induced Cardiac Pacemakers Malfunctions Analyzed at System-Level via Model Checking. IEEE Access, 2018, 6, 62107-62119.	4.2	2
62	Fault Tree Analysis And Risk Mitigation Strategies For Autonomous Systems Via Statistical Model Checking. , 2021, , .		2
63	Reliability of recursive concentrator. , 2009, , .		1
64	LCF-style Platform based on Multiway Decision Graphs. Electronic Notes in Theoretical Computer Science, 2009, 246, 3-26.	0.9	1
65	Security estimation in Streaming Protocols. , 2011, , .		1
66	Abstract property language for MDG model checking methodology. International Journal of Computer Applications in Technology, 2012, 44, 23.	0.5	1
67	Modeling discrete event system with distributions using SystemVerilog. , 2012, , .		1
68	Automatic mapping of AF3 specifications to ARM cortex-M based FRDM platfrom. , 2014, , .		1
69	Probabilistic model checking of single event transient propagation at RTL level. , 2014, , .		1
70	Optimum domain partitioning to increase functional verification coverage. , 2015, , .		1
71	Applying formal verification to early assessment of FPGA-based aerospace applications: Methodology and experience. , 2016, , .		1
72	Investigating the efficiency and accuracy of a data type reduction technique for soft error analysis. , 2016, , .		1

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73	Towards formal abstraction, modeling, and analysis of Single Event Transients at RTL. , 2016, , .		1
74	Towards code generation for ARM Cortex-M MCUs from SysML activity diagrams. , 2016, , .		1
75	Analysis of SEU Propagation in Combinational Circuits at RTL Based on Satisfiability Modulo Theories. , 2017, , .		1
76	Comprehensive analysis of sequential circuits vulnerability to transient faults using SMT. , 2017, , .		1
77	Fuzzy clustering optimized with genetic algorithms: Application for hybrid speech recognition system. , 2017, , .		1
78	Analysis of SEU propagation in sequential circuits at RTL using Satisfiability Modulo Theories. , 2017, , .		1
79	An FPGA implementation of a modified version of RED algorithm. , 0, , .		0
80	Formal Verification of System Level Designs: A GSM Vocoder Case Study. , 2007, , .		0
81	Processing APL properties to generate verification-ready MDG model. , 2009, , .		0
82	Static slicing-based pre-reduction technique for MDG model-checker. , 2009, , .		0
83	Field programmable gate array prototyping of end-around carry parallel prefix tree architectures. IET Computers and Digital Techniques, 2010, 4, 306-316.	1.2	0
84	MDGs Reduction Technique Based on the HOL Theorem Prover. , 2010, , .		0
85	Automatic verification of reduction techniques in Higher Order Logic. Formal Aspects of Computing, 2013, 25, 971-991.	1.8	0
86	Formal modeling, verification and implementation of a train control system. , 2015, , .		0
87	Special issue on contributions of computational intelligence in designing complex information systems. Computing (Vienna/New York), 2015, 97, 663-666.	4.8	0
88	Comprehensive non-functional analysis of combinational circuits vulnerability to single event transients. , 2016, , .		0
89	A low-cost camera-based transducer tracking system for freehand three-dimensional ultrasound. , 2016, , .		0
90	Investigating the efficiency of cell level hardening techniques of single event transients via SMT. , 2016, , .		0

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91	Formal Methods Based Synthesis of Single Event Transient Tolerant Combinational Circuits. Journal of Electronic Testing: Theory and Applications (JETTA), 2017, 33, 607-620.	1.2	0
92	System level SEUs propagation analysis via data flow-based reduction and quantitative model checking. , 2017, , .		0
93	Reliability Analysis of the SPARC V8 Architecture via Fault Trees and UPPAL-SMC. , 2018, , .		0
94	Probabilistic High-Level Estimation of Vulnerability and Fault Mitigation of Critical Systems Using Fault-Mitigation Trees (FMTs). , 2019, , .		0
95	On The Integration of Decision Diagrams in High Order Logic Based Theorem Provers:a Survey. Journal of Computer Science, 2007, 3, 810-817.	0.6	0
96	Technological Advances in Applied Intelligence (IEA/AIE-2018). AI Magazine, 2018, 39, 27-28.	1.6	0