Stefania Perri

List of Publications by Year in Descending Order

88 papers	856 citations	16 h-index	23 g-index
95 ext. papers	1,119 ext. citations	2 avg, IF	4.48 L-index

#	Paper	IF	Citations
88	Approximate Down-Sampling Strategy for Power-Constrained Intelligent Systems. *IEEE Access*, **2022**, 1-1	3.5	0
87	Robust and High-Performance Machine Vision System for Automatic Quality Inspection in Assembly Processes.. *Sensors*, **2022**, 22,	3.8	2
86	Aggressive Approximation of the SoftMax Function for Power-Efficient Hardware Implementations. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 1-1	3.5	1
85	Design of a real-time face detection architecture for heterogeneous systems-on-chips. *The Integration VLSI Journal*, **2020**, 74, 1-10	1.4	5
84	Approximate Multipliers With Dynamic Truncation for Energy Reduction via Graceful Quality Degradation. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 3427-3431	3.5	5
83	Energy-Efficient Architecture for CNNs Inference on Heterogeneous FPGA. *Journal of Low Power Electronics and Applications*, **2020**, 10, 1	1.7	11
82	A Parallel Connected Component Labeling Architecture for Heterogeneous Systems-on-Chip. *Electronics (Switzerland)*, **2020**, 9, 292	2.6	4
81	Parallel architecture of power-of-two multipliers for FPGAs. *IET Circuits, Devices and Systems*, **2020**, 14, 381-389	1.1	5
80	Learning Style Identification by CHAEA Junior Questionnaire and Artificial Neural Network Method: A Case Study. *Advances in Intelligent Systems and Computing*, **2020**, 326-336	0.4	
79	Reconfigurable Convolution Architecture for Heterogeneous Systems-on-Chip **2020**,		4
78	Efficient Approximate Adders for FPGA-Based Data-Paths. *Electronics (Switzerland)*, **2020**, 9, 1529	2.6	6
77	Efficient Deconvolution Architecture for Heterogeneous Systems-on-Chip. *Journal of Imaging*, **2020** , 6,	3.1	1
76	Stereo vision architecture for heterogeneous systems-on-chip. *Journal of Real-Time Image Processing*, **2020**, 17, 393-415	1.9	5
75	An embedded machine vision system for an in-line quality check of assembly processes. *Procedia Manufacturing*, **2020**, 42, 211-218	1.5	12
74	Efficient Architecture for Integral Image Computation on Heterogeneous FPGAs **2019**,		2
73	An Efficient Hardware-Oriented Single-Pass Approach for Connected Component Analysis. *Sensors*, **2019**, 19,	3.8	8
72	Automatic Microstructural Classification with Convolutional Neural Network. *Advances in Intelligent Systems and Computing*, **2019**, 170-181	0.4	2

71	Energy-Quality Scalable Adders Based on Nonzeroing Bit Truncation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 964-968	2.6	10
70	Multimodal background subtraction for high-performance embedded systems. *Journal of Real-Time Image Processing*, **2019**, 16, 1407-1423	1.9	7
69	An Efficient Connected Component Labeling Architecture for Embedded Systems. *Journal of Low Power Electronics and Applications*, **2018**, 8, 7	1.7	13
68	Design of Real-Time FPGA-based Embedded System for Stereo Vision **2018**,		8
67	**2018**,		2
66	Designing Fast Convolutional Engines for Deep Learning Applications **2018**,		5
65	Design of efficient QCA multiplexers. *International Journal of Circuit Theory and Applications*, **2016**, 44, 602-615	2	12
64	A Microchip Integrated Sensor for the Monitoring of High Concentration Photo-voltaic Solar Modules. *Procedia Engineering*, **2016**, 168, 1601-1604		2
63	An efficient hardware-oriented stereo matching algorithm. *Microprocessors and Microsystems*, **2016**, 46, 21-33	2.4	9
62	Power supply noise in accurate delay model for the sub-threshold domain. *The Integration VLSI Journal*, **2015**, 50, 127-136	1.4	1
61	Low-Leakage SRAM Wordline Drivers for the 28-nm UTBB FDSOI Technology. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 3133-3137	2.6	10
60	Fast and Wide Range Voltage Conversion in Multisupply Voltage Designs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 388-391	2.6	47
59	Exploring well configurations for voltage level converter design in 28 nm UTBB FDSOI technology **2015**,		2
58	Embedded surveillance system using background subtraction and Raspberry Pi **2015**,		6
57	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 1456-1464	3.9	16
56	Area-Delay Efficient Binary Adders in QCA. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 1174-1179	2.6	43
55	Design of Efficient Binary Comparators in Quantum-Dot Cellular Automata. *IEEE Nanotechnology Magazine*, **2014**, 13, 192-202	2.6	31
54	A novel background subtraction method based on color invariants and grayscale levels **2014**,		4

53	Design of high-speed low-power parallel-prefix adder trees in nanometer technologies. *International Journal of Circuit Theory and Applications*, **2014**, 42, 731-743	2	4
52	Analyzing noise robustness of wide fan-in dynamic logic gates under process variations. *International Journal of Circuit Theory and Applications*, **2014**, 42, 452-467	2	2
51	Gate-level body biasing technique for high-speed sub-threshold CMOS logic gates. *International Journal of Circuit Theory and Applications*, **2014**, 42, 65-70	2	32
50	Adaptive Census Transform: A novel hardware-oriented stereovision algorithm. *Computer Vision and Image Understanding*, **2013**, 117, 29-41	4.3	30
49	Low-cost FPGA stereo vision system for real time disparity maps calculation. *Microprocessors and Microsystems*, **2012**, 36, 281-288	2.4	18
48	Analytical Delay Model Considering Variability Effects in Subthreshold Domain. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2012**, 59, 168-172	3.5	25
47	Energy-efficient single-clock-cycle binary comparator. *International Journal of Circuit Theory and Applications*, **2012**, 40, 237-246	2	9
46	Low-Power Level Shifter for Multi-Supply Voltage Designs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2012**, 59, 922-926	3.5	54
45	New Methodology for the Design of Efficient Binary Addition Circuits in QCA. *IEEE Nanotechnology Magazine*, **2012**, 11, 1192-1200	2.6	32
44	Comparative analysis of yield optimized pulsed flip-flops. *Microelectronics Reliability*, **2012**, 52, 1679-1689	1.2	20
43	Design of Energy Aware Adder Circuits Considering Random Intra-Die Process Variations. *Journal of Low Power Electronics and Applications*, **2011**, 1, 97-108	1.7	7
42	Efficient memory architecture for image processing. *International Journal of Circuit Theory and Applications*, **2011**, 39, 351-356	2	9
41	Fast-squarer circuits using 3-bit-scan without overlapping bits. *International Journal of Circuit Theory and Applications*, **2011**, 39, 1037-1047	2	
40	Impact of Process Variations on Pulsed Flip-Flops: Yield Improving Circuit-Level Techniques and Comparative Analysis. *Lecture Notes in Computer Science*, **2011**, 180-189	0.9	5
39	A self-hosting configuration management system to mitigate the impact of Radiation-Induced Multi-Bit Upsets in SRAM-based FPGAs **2010**,		9
38	A new low-power high-speed single-clock-cycle binary comparator **2010**,		7
37	A fast carry chain adder for Virtex-5 FPGAs **2010**,		12
36	Impact of Process Variations on Flip-Flops Energy and Timing Characteristics **2010**,		13

35	Efficient absolute difference circuits in Virtex-5 FPGAs **2010**,		4
34	An Efficient and Low-Cost Design Methodology to Improve SRAM-Based FPGA Robustness in Space and Avionics Applications. *Lecture Notes in Computer Science*, **2009**, 74-84	0.9	4
33	Low-power split-path data-driven dynamic logic. *IET Circuits, Devices and Systems*, **2009**, 3, 303-312	1.1	12
32	Design-Space Exploration of Energy-Delay-Area Efficient Coarse-Grain Reconfigurable Datapath **2009**,		7
31	Designing High-Speed Adders in Power-Constrained Environments. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2009**, 56, 172-176	3.5	17
30	Design and Evaluation of an Energy-Delay-Area Efficient Datapath for Coarse-Grain Reconfigurable Computing Systems. *Journal of Low Power Electronics*, **2009**, 5, 326-338	1.2	6
29	A New Dynamic Logic Circuit Design for an Effective Trade-Off between Noise-Immunity, Performance and Energy Dissipation. *Lecture Notes in Computer Science*, **2009**, 277-286	0.9	2
28	Energy Efficient Coarse-Grain Reconfigurable Array for Accelerating Digital Signal Processing. *Lecture Notes in Computer Science*, **2009**, 297-306	0.9	
27	High-performance noise-tolerant circuit techniques for CMOS dynamic logic. *IET Circuits, Devices and Systems*, **2008**, 2, 537	1.1	16
26	A high flexible Early-Late Gate bit synchronizer in FPGA-based software defined radios **2008**,		9
25	Fast Low-Cost Implementation of Single-Clock-Cycle Binary Comparator. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2008**, 55, 1239-1243	3.5	20
24	A matrix product accelerator for field programmable systems on chip. *Microprocessors and Microsystems*, **2008**, 32, 53-67	2.4	7
23	A programmable carrier phase independent symbol timing recovery circuit for QPSK/OQPSK signals. *Microprocessors and Microsystems*, **2008**, 32, 437-446	2.4	6
22	VLSI implementations of efficient isotropic flexible 2D convolvers. *IET Circuits, Devices and Systems*, **2007**, 1, 263	1.1	6
21	Parallel Multipliers using 3-Bit-Scan without Overlapping Bits **2007**,		1
20	**2007**,		2
19	A New Reconfigurable Coarse-Grain Architecture for Multimedia Applications **2007**,		14
18	MORA: A New Coarse-Grain Reconfigurable Array for High Throughput Multimedia Processing **2007** , 159-168		11

17	SIMD MULTIPLIERS FOR ACCELERATING EMBEDDED PROCESSORS IN FPGAs. *Journal of Circuits, Systems and Computers*, **2006**, 15, 537-550	0.9	1
16	SAD-Based Stereo Matching Circuit for FPGAs **2006**,		16
15	An Efficient Bit-Detection and Timing Recovery Circuit for FPGAs **2006**,		5
14	Techniques for Leakage Energy Reduction in Deep Submicrometer Cache Memories. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2006**, 14, 1238-1249	2.6	17
13	Microprocessor-based FPGA implementation of SPIHT image compression subsystems. *Microprocessors and Microsystems*, **2005**, 29, 299-305	2.4	10
12	A high-performance fully reconfigurable FPGA-based 2D convolution processor. *Microprocessors and Microsystems*, **2005**, 29, 381-391	2.4	28
11	EFFICIENT RECONFIGURABLE MANCHESTER ADDERS FOR LOW-POWER MEDIA PROCESSING. *Journal of Circuits, Systems and Computers*, **2005**, 14, 57-63	0.9	
10	Variable precision arithmetic circuits for FPGA-based multimedia processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2004**, 12, 995-999	2.6	9
9	A high-speed energy-efficient 64-bit reconfigurable binary adder. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2003**, 11, 939-943	2.6	10
8	An efficient self-timed adder realized using conventional CMOS standard cells. *International Journal of Electronics*, **2003**, 90, 413-422	1.2	
7	64-bit reconfigurable adder for low power media processing. *Electronics Letters*, **2002**, 38, 397	1.1	10
6	VLSI circuits for low-power high-speed asynchronous addition. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2002**, 10, 608-613	2.6	4
5	High performance mixed-logic asynchronous datapaths with overlapped execution circuits. *International Journal of Electronics*, **2000**, 87, 1193-1208	1.2	2
4	Area-time-power tradeoff in cellular arrays VLSI implementations. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2000**, 8, 614-624	2.6	2
3	VLSI Implementation of a Low-Power High-Speed Self-Timed Adder. *Lecture Notes in Computer Science*, **2000**, 195-204	0.9	2
2	Hybrid carry-select statistical carry look-ahead adder. *Electronics Letters*, **1999**, 35, 549	1.1	2
1	A new high performance circuit for statistical carry lookahead addition. *International Journal of Electronics*, **1999**, 86, 713-722	1.2	4