Stefania Perri

List of Publications by Year
in descending order

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94 papers	1,284 citations	430442 18 h-index	476904 29 g-index
95 all docs	95 docs citations	95 times ranked	859 citing authors

#	Article	IF	Citations
1	Low-Power Level Shifter for Multi-Supply Voltage Designs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 922-926.	2.2	84
2	Fast and Wide Range Voltage Conversion in Multisupply Voltage Designs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 388-391.	2.1	79
3	Area-Delay Efficient Binary Adders in QCA. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1174-1179.	2.1	55
4	New Methodology for the Design of Efficient Binary Addition Circuits in QCA. IEEE Nanotechnology Magazine, 2012, 11, 1192-1200.	1.1	44
5	Gateâ€level body biasing technique for highâ€speed subâ€threshold CMOS logic gates. International Journal of Circuit Theory and Applications, 2014, 42, 65-70.	1.3	44
6	Analytical Delay Model Considering Variability Effects in Subthreshold Domain. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 168-172.	2.2	39
7	A high-performance fully reconfigurable FPGA-based 2D convolution processor. Microprocessors and Microsystems, 2005, 29, 381-391.	1.8	38
8	Design of Efficient Binary Comparators in Quantum-Dot Cellular Automata. IEEE Nanotechnology Magazine, 2014, 13, 192-202.	1.1	38
9	Adaptive Census Transform: A novel hardware-oriented stereovision algorithm. Computer Vision and Image Understanding, 2013, 117, 29-41.	3.0	33
10	Fast Low-Cost Implementation of Single-Clock-Cycle Binary Comparator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 1239-1243.	2.2	31
11	Comparative analysis of yield optimized pulsed flip-flops. Microelectronics Reliability, 2012, 52, 1679-1689.	0.9	28
12	Techniques for Leakage Energy Reduction in Deep Submicrometer Cache Memories. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 1238-1249.	2.1	27
13	High-performance noise-tolerant circuit techniques for CMOS dynamic logic. IET Circuits, Devices and Systems, 2008, 2, 537.	0.9	26
14	Low-power split-path data-driven dynamic logic. IET Circuits, Devices and Systems, 2009, 3, 303-312.	0.9	26
15	A New Reconfigurable Coarse-Grain Architecture for Multimedia Applications. , 2007, , .		24
16	Designing High-Speed Adders in Power-Constrained Environments. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 172-176.	2.2	23
17	Low-cost FPGA stereo vision system for real time disparity maps calculation. Microprocessors and Microsystems, 2012, 36, 281-288.	1.8	23
18	An embedded machine vision system for an in-line quality check of assembly processes. Procedia Manufacturing, 2020, 42, 211-218.	1.9	22

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19	SAD-Based Stereo Matching Circuit for FPGAs. , 2006, , .		21
20	Energy-Quality Scalable Adders Based on Nonzeroing Bit Truncation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 964-968.	2.1	20
21	A fast carry chain adder for Virtex-5 FPGAs. , 2010, , .		18
22	Over/Undershooting Effects in Accurate Buffer Delay Model for Sub-Threshold Domain. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1456-1464.	3.5	18
23	Energyâ€efficient singleâ€clockâ€cycle binary comparator. International Journal of Circuit Theory and Applications, 2012, 40, 237-246.	1.3	17
24	An Efficient Connected Component Labeling Architecture for Embedded Systems. Journal of Low Power Electronics and Applications, 2018, 8, 7.	1.3	17
25	A new low-power high-speed single-clock-cycle binary comparator. , 2010, , .		16
26	Impact of Process Variations on Flip-Flops Energy and Timing Characteristics. , 2010, , .		16
27	Energy-Efficient Architecture for CNNs Inference on Heterogeneous FPGA. Journal of Low Power Electronics and Applications, 2020, 10, 1.	1.3	16
28	A matrix product accelerator for field programmable systems on chip. Microprocessors and Microsystems, 2008, 32, 53-67.	1.8	15
29	Design of efficient QCA multiplexers. International Journal of Circuit Theory and Applications, 2016, 44, 602-615.	1.3	15
30	A high-speed energy-efficient 64-bit reconfigurable binary adder. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2003, 11, 939-943.	2.1	14
31	Microprocessor-based FPGA implementation of SPIHT image compression subsystems. Microprocessors and Microsystems, 2005, 29, 299-305.	1.8	14
32	An Efficient Hardware-Oriented Single-Pass Approach for Connected Component Analysis. Sensors, 2019, 19, 3055.	2.1	14
33	64-bit reconfigurable adder for low power media processing. Electronics Letters, 2002, 38, 397.	0.5	13
34	Efficient Approximate Adders for FPGA-Based Data-Paths. Electronics (Switzerland), 2020, 9, 1529.	1.8	13
35	Approximate Multipliers With Dynamic Truncation for Energy Reduction via Graceful Quality Degradation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3427-3431.	2.2	13
36	Variable precision arithmetic circuits for FPGA-based multimedia processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2004, 12, 995-999.	2.1	12

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37	A high flexible Early-Late Gate bit synchronizer in FPGA-based software defined radios. , 2008, , .		12
38	Design of Real-Time FPGA-based Embedded System for Stereo Vision. , 2018, , .		12
39	A self-hosting configuration management system to mitigate the impact of Radiation-Induced Multi-Bit Upsets in SRAM-based FPGAs. , 2010, , .		11
40	Efficient memory architecture for image processing. International Journal of Circuit Theory and Applications, 2011, 39, 351-356.	1.3	11
41	Low-Leakage SRAM Wordline Drivers for the 28-nm UTBB FDSOI Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 3133-3137.	2.1	11
42	Stereo vision architecture for heterogeneous systems-on-chip. Journal of Real-Time Image Processing, 2020, 17, 393-415.	2.2	11
43	A programmable carrier phase independent symbol timing recovery circuit for QPSK/OQPSK signals. Microprocessors and Microsystems, 2008, 32, 437-446.	1.8	10
44	Design-Space Exploration of Energy-Delay-Area Efficient Coarse-Grain Reconfigurable Datapath. , 2009, , .		10
45	Impact of Process Variations on Pulsed Flip-Flops: Yield Improving Circuit-Level Techniques and Comparative Analysis. Lecture Notes in Computer Science, 2011, , 180-189.	1.0	10
46	An efficient hardware-oriented stereo matching algorithm. Microprocessors and Microsystems, 2016, 46, 21-33.	1.8	10
47	Design and Evaluation of an Energy-Delay-Area Efficient Datapath for Coarse-Grain Reconfigurable Computing Systems. Journal of Low Power Electronics, 2009, 5, 326-338.	0.6	10
48	Design of Energy Aware Adder Circuits Considering Random Intra-Die Process Variations. Journal of Low Power Electronics and Applications, 2011, 1, 97-108.	1.3	9
49	Embedded surveillance system using background subtraction and Raspberry Pi. , 2015, , .		9
50	Multimodal background subtraction for high-performance embedded systems. Journal of Real-Time Image Processing, 2019, 16, 1407-1423.	2.2	8
51	An Efficient Bit-Detection and Timing Recovery Circuit for FPGAs. , 2006, , .		7
52	An efficient and optimized FPGA Feedback M-PSK Symbol Timing Recovery Architecture based on the Gardner Timing Error Detector. , 2007, , .		7
53	An Efficient and Low-Cost Design Methodology to Improve SRAM-Based FPGA Robustness in Space and Avionics Applications. Lecture Notes in Computer Science, 2009, , 74-84.	1.0	7
54	Efficient absolute difference circuits in Virtex-5 FPGAs. , 2010, , .		7

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55	Design of highâ€speed lowâ€power parallelâ€prefix adder trees in nanometer technologies. International Journal of Circuit Theory and Applications, 2014, 42, 731-743.	1.3	7
56	Design of a real-time face detection architecture for heterogeneous systems-on-chips. The Integration VLSI Journal, 2020, 74, 1-10.	1.3	7
57	A Parallel Connected Component Labeling Architecture for Heterogeneous Systems-on-Chip. Electronics (Switzerland), 2020, 9, 292.	1.8	7
58	Parallel architecture of powerâ€ofâ€two multipliers for FPGAs. IET Circuits, Devices and Systems, 2020, 14, 381-389.	0.9	7
59	Aggressive Approximation of the SoftMax Function for Power-Efficient Hardware Implementations. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1652-1656.	2.2	7
60	Design of Flexible Hardware Accelerators for Image Convolutions and Transposed Convolutions. Journal of Imaging, 2021, 7, 210.	1.7	7
61	Area-time-power tradeoff in cellular arrays VLSI implementations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2000, 8, 614-624.	2.1	6
62	VLSI circuits for low-power high-speed asynchronous addition. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 608-613.	2.1	6
63	VLSI implementations of efficient isotropic flexible 2D convolvers. IET Circuits, Devices and Systems, 2007, 1, 263.	0.9	6
64	Analyzing noise robustness of wide fanâ€in dynamic logic gates under process variations. International Journal of Circuit Theory and Applications, 2014, 42, 452-467.	1.3	6
65	Designing Fast Convolutional Engines for Deep Learning Applications. , 2018, , .		6
66	Reconfigurable Convolution Architecture for Heterogeneous Systems-on-Chip. , 2020, , .		6
67	A novel background subtraction method based on color invariants and grayscale levels. , 2014, , .		5
68	Efficient Deconvolution Architecture for Heterogeneous Systems-on-Chip. Journal of Imaging, 2020, 6, 85.	1.7	5
69	Approximate Down-Sampling Strategy for Power-Constrained Intelligent Systems. IEEE Access, 2022, 10, 7073-7081.	2.6	5
70	Robust and High-Performance Machine Vision System for Automatic Quality Inspection in Assembly Processes. Sensors, 2022, 22, 2839.	2.1	5
71	A new high performance circuit for statistical carry lookahead addition. International Journal of Electronics, 1999, 86, 713-722.	0.9	4
72	High performance mixed-logic asynchronous datapaths with overlapped execution circuits. International Journal of Electronics, 2000, 87, 1193-1208.	0.9	3

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73	Exploring well configurations for voltage level converter design in 28 nm UTBB FDSOI technology. , 2015, , .		3
74	Efficient Architecture for Integral Image Computation on Heterogeneous FPGAs. , 2019, , .		3
75	Automatic Microstructural Classification with Convolutional Neural Network. Advances in Intelligent Systems and Computing, 2019, , 170-181.	0.5	3
76	VLSI Implementation of a Low-Power High-Speed Self-Timed Adder. Lecture Notes in Computer Science, 2000, , 195-204.	1.0	3
77	Hybrid carry-select statistical carry look-ahead adder. Electronics Letters, 1999, 35, 549.	0.5	2
78	A Microchip Integrated Sensor for the Monitoring of High Concentration Photo-voltaic Solar Modules. Procedia Engineering, 2016, 168, 1601-1604.	1.2	2
79	Connected Component Analysis for Traffic Sign Recognition Embedded Processing Systems. , 2018, , .		2
80	A New Dynamic Logic Circuit Design for an Effective Trade-Off between Noise-Immunity, Performance and Energy Dissipation. Lecture Notes in Computer Science, 2009, , 277-286.	1.0	2
81	SIMD MULTIPLIERS FOR ACCELERATING EMBEDDED PROCESSORS IN FPGAs. Journal of Circuits, Systems and Computers, 2006, 15, 537-550.	1.0	1
82	Parallel Multipliers using 3-Bit-Scan without Overlapping Bits. , 2007, , .		1
83	Power supply noise in accurate delay model for the sub-threshold domain. The Integration VLSI Journal, 2015, 50, 127-136.	1.3	1
84	An Efficient Convolution Engine based on the Ã€-trous Spatial Pyramid Pooling. , 2020, , .		1
85	Energy Efficient Coarse-Grain Reconfigurable Array for Accelerating Digital Signal Processing. Lecture Notes in Computer Science, 2009, , 297-306.	1.0	1
86	Learning Style Identification by CHAEA Junior Questionnaire and Artificial Neural Network Method: A Case Study. Advances in Intelligent Systems and Computing, 2020, , 326-336.	0.5	1
87	Runtime Reconfigurable Hardware Accelerator for Energy-Efficient Transposed Convolutions. , 2022, , .		1
88	An efficient self-timed adder realized using conventional CMOS standard cells. International Journal of Electronics, 2003, 90, 413-422.	0.9	0
89	EFFICIENT RECONFIGURABLE MANCHESTER ADDERS FOR LOW-POWER MEDIA PROCESSING. Journal of Circuits, Systems and Computers, 2005, 14, 57-63.	1.0	0
90	Design and Implementation of a 90nm Low bit-rate Image Compression Core. , 2007, , .		0

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91	VLSI Circuits for Accurate Motion Estimation. , 2010, , .		0
92	Fastâ€squarer circuits using 3â€bitâ€scan without overlapping bits. International Journal of Circuit Theory and Applications, 2011, 39, 1037-1047.	1.3	0
93	Editorial for the Special Issue on â€œQuantum-Dot Cellular Automata (QCA) and Low Power Applicationâ€. Journal of Low Power Electronics and Applications, 2018, 8, 40.	1.3	0
94	A High-Performance and Power-Efficient SIMD Convolution Engine for FPGAs. , 2020, , .		0