Sumin Choi

List of Publications by Year
in descending order

26 papers	193 citations	1937685 4 h-index	2272923 4 g-index
26 all docs	26 docs citations	26 times ranked	152 citing authors

#	Article	IF	Citations
1	A Novel Eye-Diagram Estimation Method for Pulse Amplitude Modulation With N-Level (PAM-N) on Stacked Through-Silicon Vias. IEEE Transactions on Electromagnetic Compatibility, 2019, 61, 1198-1206.	2.2	8
2	Design and Analysis of a 10 Gbps USB 3.2 Gen 2 Type-C Connector for TV Set-Top Box. , 2019, , .		4
3	Modeling and Analysis of TSV Noise Coupling Effects on RF LC-VCO and Shielding Structures in 3D IC. IEEE Transactions on Electromagnetic Compatibility, 2018, 60, 1939-1947.	2.2	14
4	Signal Integrity Design and Analysis of Silicon Interposer for GPU-Memory Channels in High-Bandwidth Memory Interface. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 1658-1671.	2.5	40
5	A Novel Stochastic Model-Based Eye-Diagram Estimation Method for 8B/10B and TMDS-Encoded High-Speed Channels. IEEE Transactions on Electromagnetic Compatibility, 2018, 60, 1510-1519.	2.2	13
6	Eye-diagram estimation with stochastic model for 8B/10B encoded high-speed channel. , 2018, , .		2
7	Estimation and analysis of crosstalk effects in high-bandwidth memory channel. , 2018, , .		0
8	Statistical eye-diagram estimation method for high-speed channel with N-tap decision feedback equalizer (DFE). , 2018, , .		2
9	Signal Integrity Analysis of Silicon/Glass/Organic Interposers for 2.5D/3D Interconnects. , 2017, , .		9
10	Signal and power integrity (SI/PI) analysis of heterogeneous integration using embedded multi-die interconnect bridge (EMIB) technology for high bandwidth memory (HBM). , 2017, , .		4
11	Eye-Diagram Estimation Methods for Voltage-and Probability-Dependent PAM-4 Signal on Stacked Through-Silicon Vias (TSVs). , 2017, , .		4
12	Design and Analysis of Power Distribution Network (PDN) for High Bandwidth Memory (HBM) Interposer in 2.5D Terabyte/s Bandwidth Graphics Module. , 2016, , .		24
13	Eye-diagram estimation using equivalent circuit model of coupled microstrip channel on high-speed and wide I/O Channel for 2.5D and 3D IC. , 2016, , .		2
14	Signal Integrity of Bump-Less High-Speed through Silicon Via Channel for Terabyte/s Bandwidth 2.5D IC. , 2016, , .		3
15	Power distribution network (PDN) design and analysis of a single and double-sided high bandwidth memory (HBM) interposer for 2.5D Terabtye/s bandwidth system. , 2016, , .		13
16	Modeling and analysis of high-speed through silicon via (TSV) channel and defects. , 2016, , .		3
17	Eye-diagram estimation and analysis of High-Bandwidth Memory (HBM) interposer channel with crosstalk reduction schemes on 2.5D and 3D IC. , 2016, , .		5
18	Design of an On-Interposer Passive Equalizer for High Bandwidth Memory (HBM) with 30Gbps Data Transmission. , 2016, , .		1

#	Article	IF	Citations
19	Electrical performance of high bandwidth memory (HBM) interposer channel in terabyte/s bandwidth graphics module. , 2015, , .		9
20	Design optimization of high bandwidth memory (HBM) interposer considering signal integrity. , 2015, , .		21
21	Crosstalk-included eye-diagram estimation for high-speed silicon, organic, and glass interposer channels on 2.5D/3D IC. , 2015, , .		2
22	Design of an on-interposer passive equalizer embedded on a ground plane for 30Gbps serial data transmission. , 2015, , .		1
23	Shielding structures for through silicon via (TSV) to active circuit noise coupling in 3D IC. , 2015, , .		4
24	Signal integrity design of bump-less interconnection for high-speed signaling in 2.5D and 3D IC. , 2015, , .		0
25	Crosstalk included eye diagram estimation of high-speed and wide I/O interposer channel for 2.5D / 3D IC. , 2014, , .		5
26	Electrical characterization of bump-less high speed channel on silicon, organic and glass interposer. , 2014, , .		0