Chang Cai

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/777565/publications.pdf

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11	59	1684188 5	1588992 8
papers	citations	h-index	g-index

11	11	11	42
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	SEU sensitivity and large spacing TMR efficiency of Kintex-7 and Virtex-7 FPGAs. Science China Information Sciences, 2022, 65, 1.	4.3	1
2	SEU Tolerance Efficiency of Multiple Layout-Hardened 28 nm DICE D Flip-Flops. Electronics (Switzerland), 2022, 11, 972.	3.1	5
3	Characterization and Classification of Heavy Ion Induced Failures in FPGA-based Logical Circuits. , 2021, , .		0
4	Verification of SEU resistance in 65Ânm high-performance SRAM with dual DICE interleaving and EDAC mitigation strategies. Nuclear Science and Techniques/Hewuli, 2021, 32, 1.	3.4	4
5	Multiple Layout-Hardening Comparison of SEU-Mitigated Filp-Flops in 22-nm UTBB FD-SOI Technology. IEEE Transactions on Nuclear Science, 2020, 67, 374-381.	2.0	12
6	Evaluation Method of Heavy-Ion-Induced Single-Event Upset in 3D-Stacked SRAMs. Electronics (Switzerland), 2020, 9, 1230.	3.1	0
7	Characterization of Heavy Ion Induced SET Features in 22-nm FD-SOI Testing Circuits. IEEE Access, 2020, 8, 45378-45389.	4.2	6
8	Design and verification of universal evaluation system for single event effect sensitivity measurement in very-large-scale integrated circuits. IEICE Electronics Express, 2019, 16, 20190196-20190196.	0.8	5
9	Heavy-ion and pulsed-laser single event effects in 130-nm CMOS-based thin/thick gate oxide anti-fuse PROMs. Nuclear Science and Techniques/Hewuli, 2019, 30, 1.	3.4	4
10	Heavy-Ion Induced Single Event Upsets in Advanced 65 nm Radiation Hardened FPGAs. Electronics (Switzerland), 2019, 8, 323.	3.1	13
11	SEE Sensitivity Evaluation for Commercial 16 nm SRAM-FPGA. Electronics (Switzerland), 2019, 8, 1531.	3.1	9