Subramanian S Iyer

List of Publications by Year
in descending order

38	418	1163117 8	996975 15
papers	citations	h-index	g-index

39	39	39	289
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Accuracy and Resiliency of Analog Compute-in-Memory Inference Engines. ACM Journal on Emerging Technologies in Computing Systems, 2022, 18, 1-23.	2.3	1
2	Chips, Dies, Chiplets and Dielets and Heterogeneous Integration. , 2022, , .		0
3	Characterization and Design Improvement of a High Bandwidth, High Frequency Flexible Connector for Signal Delivery. , 2022, , .		0
4	Functional Demonstration of < 0.4-pJ/bit, 9.8 Î¼m Fine-Pitch Dielet-to-Dielet Links for Advanced Packaging using Silicon Interconnect Fabric. , 2022, , .		4
5	RF Characterization on Nb-based Superconducting Silicon Interconnect Fabric for Future Large Scale Quantum Applications. , 2022, , .		0
6	TSV-less Power Delivery for Wafer-scale Assemblies and Interposers. , 2022, , .		1
7	Recess Effect Study and Process Optimization of Sub-10 Î¼m Pitch Die-to-wafer Hybrid Bonding. , 2022, , .		7
8	Smartphone App-Enabled Flex sEMG Patch using FOWLP. , 2022, , .		2
9	Experimental demonstration of pressure-driven flash boiling for transient two-phase cooling. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, , 1-1.	2.5	2
10	Nb-based superconducting silicon interconnect fabric for cryogenic electronics. Quantum Science and Technology, 2021, 6, 025014.	5.8	5
11	Method and software platform for electronic COTS parts reliability estimation in space applications. Proceedings of the Institution of Mechanical Engineers, Part O: Journal of Risk and Reliability, 2021, 235, 744-760.	0.7	1
12	Silicon-Interconnect Fabric for Fine-Pitch (â‰¤10 Î¼m) Heterogeneous Integration. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 727-738.	2.5	25
13	I/O Architecture, Substrate Design, and Bonding Process for a Heterogeneous Dielet-Assembly based Waferscale Processor. , 2021, , .		2
14	Copper to gold thermal compression bonding in heterogenous wafer-scale systems. , 2021, , .		3
15	Flexible Connectors and PCB Segmentation for Signaling and Power Delivery in Wafer-Scale Systems. , 2021, , .		2
16	Non-Volatile Wideband Frequency Tuning of a Ring-Oscillator by Charge Trapping in High-k Gate Dielectric in 22nm CMOS. IEEE Electron Device Letters, 2021, 42, 110-113.	3.9	0
17	Co-optimizing signaling protocol with semiconductor and packaging technology. , 2021, , .		1
18	Fine-Pitch (â‰¤ 10 Âµm) Nb-based Superconducting Silicon Interconnect Fabric for Large-Scale Quantum System Application. , 2021, , .		1

#	Article	IF	Citations
19	A Signaling Figure of Merit (s-FoM) for Advanced Packaging. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 1758-1761.	2.5	8
20	Charge-Trap Transistors for CMOS-Only Analog Memory. IEEE Transactions on Electron Devices, 2019, 66, 4183-4187.	3.0	18
21	Dynamic Thermal Management Of Silicon Interconnect Fabric Using Flash Cooling. , 2019, , .		9
22	Reliability Evaluation of Silicon Interconnect Fabric Technology. , 2019, , .		1
23	Design Optimization and Modeling of Charge Trap Transistors (CTTs) in 14 nm FinFET Technologies. IEEE Electron Device Letters, 2019, 40, 1100-1103.	3.9	15
24	Architecting Waferscale Processors - A GPU Case Study. , 2019, , .		25
25	PowerTherm Attach Process for Power Delivery and Heat Extraction in the Silicon-Interconnect Fabric Using Thermocompression Bonding. , 2019, , .		8
26	A Case for Packageless Processors. , 2018, , .		15
27	Demonstration of a Heterogeneously Integrated System-on-Wafer (SoW) Assembly. , 2018, , .		13
28	Reliability challenges in advance packaging. , 2018, , .		3
29	Characterization of Fine-Pitch Interconnections (â‰ 10 Î¼m) on Silicon Interconnect Fabric for Heterogeneous Integration. International Symposium on Microelectronics, 2018, 2018, 000556-000560.	0.0	1
30	Assessing Benefits of a Buried Interconnect Layer in Digital Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 346-350.	2.7	6
31	Charge Trap Transistor (CTT): An Embedded Fully Logic-Compatible Multiple-Time Programmable Non-Volatile Memory Element for High- k -Metal-Gate CMOS Technologies. IEEE Electron Device Letters, 2017, 38, 44-47.	3.9	37
32	Three-dimensional wafer scale integration for ultra-large-scale cognitive systems. , 2017, , .		3
33	Latency, Bandwidth and Power Benefits of the SuperCHIPS Integration Scheme. , 2017, , .		33
34	Advanced Packaging and Heterogeneous Integration to Reboot Computing. , 2017, , .		1
35	Three-Dimensional Dynamic Random Access Memories Using Through-Silicon-Vias. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2016, 6, 373-384.	3.6	13
36	The Impact of Self-Heating on Charge Trapping in High-<inline-formula> <tex-math notation="LaTeX">k </tex-math></inline-formula>-Metal-Gate nFETs. IEEE Electron Device Letters, 2016, 37, 88-91.	3.9	27

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37	Heterogeneous Integration for Performance and Scaling. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2016, 6, 973-982.	2.5	107
38	Three-Dimensional Integration: A Tutorial for Designers. IEEE Solid-State Circuits Magazine, 2015, 7, 63-74.	0.4	18