Yee-Chia Yeo

List of Publications by Year
in descending order

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370 papers	7,280 citations	61945 43 h-index	88593 70 g-index
370 all docs	370 docs citations	370 times ranked	4406 citing authors

#	Article	IF	Citations
1	Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology. Journal of Applied Physics, 2002, 92, 7266-7271.	1.1	393
2	Tunneling Field-Effect Transistor: Capacitance Components and Modeling. IEEE Electron Device Letters, 2010, 31, 752-754.	2.2	213
3	Electronic band structure and effective mass parameters of Ge1-xSnx alloys. Journal of Applied Physics, 2012, 112, .	1.1	194
4	MOSFET gate leakage modeling and selection guide for alternative gate dielectrics based on leakage considerations. IEEE Transactions on Electron Devices, 2003, 50, 1027-1035.	1.6	192
5	Direct tunneling leakage current and scalability of alternative gate dielectrics. Applied Physics Letters, 2002, 81, 2091-2093.	1.5	184
6	Device physics and design of germanium tunneling field-effect transistor with source and drain engineering for low power and high performance applications. Journal of Applied Physics, 2008, 103, .	1.1	167
7	Effects of high-/spl kappa/ gate dielectric materials on metal and silicon gate workfunctions. IEEE Electron Device Letters, 2002, 23, 342-344.	2.2	159
8	Device physics and design of double-gate tunneling field-effect transistor by silicon film thickness optimization. Applied Physics Letters, 2007, 90, 263507.	1.5	130
9	Fermi Pinning-Induced Thermal Instability of Metal-Gate Work Functions. IEEE Electron Device Letters, 2004, 25, 337-339.	2.2	118
10	Lattice strain analysis of transistor structures with siliconâ€“germanium and siliconâ€“carbon sourceâˆ•drain stressors. Applied Physics Letters, 2005, 86, 093102.	1.5	103
11	Nonvolatile Flash Memory Device Using Ge Nanocrystals Embedded in HfAlO High-<tex>$kappa$</tex>Tunneling and Control Oxides: Device Fabrication and Electrical Performance. IEEE Transactions on Electron Devices, 2004, 51, 1840-1848.	1.6	97
12	Tunneling Field-Effect Transistor: Effect of Strain and Temperature on Tunneling Current. IEEE Electron Device Letters, 2009, 30, 981-983.	2.2	96
13	Dual-metal gate CMOS technology with ultrathin silicon nitride gate dielectric. IEEE Electron Device Letters, 2001, 22, 227-229.	2.2	94
14	A Variational Approach to the Two-Dimensional Nonlinear Poisson's Equation for the Modeling of Tunneling Transistors. IEEE Electron Device Letters, 2008, 29, 1252-1255.	2.2	94
15	Germanium–Tin (GeSn) p-Channel MOSFETs Fabricated on (100) and (111) Surface Orientations With Sub-400 <formula formulatype="inline"><tex Notation="TeX">$^{circ}hbox{C} hbox{Si}_{2}hbox{H}_{6}$</tex> </formula> Passivation. IEEE Electron Device Letters, 2013, 34, 339-341.	2.2	94
16	Sulfur-Induced PtSi:C/Si:C Schottky Barrier Height Lowering for Realizing N-Channel FinFETs With Reduced External Resistance. IEEE Electron Device Letters, 2009, 30, 472-474.	2.2	92
17	Device Design and Scalability of a Double-Gate Tunneling Field-Effect Transistor with Siliconâ€“Germanium Source. Japanese Journal of Applied Physics, 2008, 47, 2593.	0.8	89
18	Device physics and guiding principles for the design of double-gate tunneling field effect transistor with silicon-germanium source heterojunction. Applied Physics Letters, 2007, 91, .	1.5	88

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19	High-speed photo detection at two-micron-wavelength: technology enablement by GeSn/Ge multiple-quantum-well photodiode on 300 mm Si substrate. Optics Express, 2019, 27, 5798.	1.7	82
20	Two-micron-wavelength germanium-tin photodiodes with low dark current and gigahertz bandwidth. Optics Express, 2017, 25, 15818.	1.7	78
21	Direct-tunneling gate leakage current in double-gate and ultrathin body MOSFETs. IEEE Transactions on Electron Devices, 2002, 49, 2288-2295.	1.6	74
22	Critical thickness for strain relaxation of Ge1â^'xSnx (xâ€‰â‰¤â€‰0.17) grown by molecular beam epitaxy on Ge(001). Applied Physics Letters, 2015, 106, .	1.5	70
23	Metal gate technology for nanoscale transistorsâ€”material selection and process integration issues. Thin Solid Films, 2004, 462-463, 34-41.	0.8	68
24	Finite-element study of strain distribution in transistor with siliconâ€“germanium source and drain regions. Applied Physics Letters, 2005, 86, 023103.	1.5	68
25	A fast measurement technique of MOSFETI/sub d/-V/sub g/ characteristics. IEEE Electron Device Letters, 2006, 27, 55-57.	2.2	64
26	IIIâ€“V Multiple-Gate Field-Effect Transistors With High-Mobility $hbox{In}_{0.7}hbox{Ga}_{0.3}hbox{As}$ Channel and Epi-Controlled Retrograde-Doped Fin. IEEE Electron Device Letters, 2011, 32, 146-148.	2.2	63
27	Relaxed and Strained Patterned Germanium-Tin Structures: A Raman Scattering Study. ECS Journal of Solid State Science and Technology, 2013, 2, P138-P145.	0.9	62
28	Suppression of dark current in germanium-tin on silicon p-i-n photodiode by a silicon surface passivation technique. Optics Express, 2015, 23, 18611.	1.7	59
29	Silicon-based tunneling field-effect transistor with elevated germanium source formed on (110) silicon substrate. Applied Physics Letters, 2011, 98, 153502.	1.5	58
30	Wide $V_{m fb}$ and $V_{m th}$ Tunability for Metal-Gated MOS Devices With HfLaO Gate Dielectrics. IEEE Electron Device Letters, 2007, 28, 258-260.	2.2	57
31	Silane and Ammonia Surface Passivation Technology for High-Mobility $hbox{In}_{0.53}hbox{Ga}_{0.47}hbox{As}$ MOSFETs. IEEE Transactions on Electron Devices, 2010, 57, 973-979.	1.6	57
32	A Simulation Study of Graphene-Nanoribbon Tunneling FET With Heterojunction Channel. IEEE Electron Device Letters, 2010, 31, 555-557.	2.2	57
33	Lattice-Mismatched $hbox{In}_{0.4}hbox{Ga}_{0.6} hbox{As}$ Source/Drain Stressors With In Situ Doping for Strained $hbox{In}_{0.53}hbox{Ga}_{0.47}hbox{As}$ Channel n-MOSFETs. IEEE Electron Device Letters, 2009, 30, 805-807.	2.2	53
34	Germaniumâ€“Tin P-Channel Tunneling Field-Effect Transistor: Device Design and Technology Demonstration. IEEE Transactions on Electron Devices, 2013, 60, 4048-4056.	1.6	52
35	A Dual-Metal Gate Integration Process for CMOS With Sub-1-nm EOT<tex>$hbox HfO_2$</tex>by Using HfN Replacement Gate. IEEE Electron Device Letters, 2004, 25, 580-582.	2.2	51
36	Ballistic Transport Performance of Silicane and Germanane Transistors. IEEE Transactions on Electron Devices, 2014, 61, 1590-1598.	1.6	51

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37	Formation of Ge nanocrystals in HfAlO high-k dielectric and application in memory device. Applied Physics Letters, 2004, 84, 5407-5409.	1.5	50
38	New materials for post-Si computing: Ge and GeSn devices. MRS Bulletin, 2014, 39, 678-686.	1.7	50
39	Aluminum oxynitride interfacial passivation layer for high-permittivity gate dielectric stack on gallium arsenide. Applied Physics Letters, 2006, 89, 202903.	1.5	48
40	n-MOSFET With Siliconâ€“Carbon Source/Drain for Enhancement of Carrier Transport. IEEE Transactions on Electron Devices, 2007, 54, 249-256.	1.6	48
41	Germanium-Tin on Si Avalanche Photodiode: Device Design and Technology Demonstration. IEEE Transactions on Electron Devices, 2015, 62, 128-135.	1.6	48
42	Tin surface segregation, desorption, and island formation during post-growth annealing of strained epitaxial Ge1â^'xSnx layer on Ge(001) substrate. Applied Surface Science, 2014, 321, 240-244.	3.1	47
43	Electrical Characteristics of Memory Devices With a High-$k$$hbox{HfO}_{2}$ Trapping Layer and Dual $hbox{SiO}_{2}/hbox{Si}_{3}hbox{N}_{4}$ Tunneling Layer. IEEE Transactions on Electron Devices, 2007, 54, 2699-2705.	1.6	46
44	Floating-base germanium-tin heterojunction phototransistor for high-efficiency photodetection in short-wave infrared range. Optics Express, 2017, 25, 18502.	1.7	44
45	Sub-0.1-eV Effective Schottky-Barrier Height for NiSi on n-Type Si (100) Using Antimony Segregation. IEEE Electron Device Letters, 2007, 28, 703-705.	2.2	43
46	Ge0.97Sn0.03 p-channel metal-oxide-semiconductor field-effect transistors: Impact of Si surface passivation layer thickness and post metal annealing. Journal of Applied Physics, 2013, 114, 044510.	1.1	43
47	Towards direct band-to-band tunneling in P-channel tunneling field effect transistor (TFET): Technology enablement by Germanium-tin (GeSn). , 2012, , .		42
48	Germanium-tin n-channel tunneling field-effect transistor: Device physics and simulation study. Journal of Applied Physics, 2013, 113, .	1.1	42
49	Nickel-Silicide:Carbon Contact Technology for N-Channel MOSFETs With Siliconâ€“Carbon Source/Drain. IEEE Electron Device Letters, 2008, 29, 89-92.	2.2	41
50	In[sub 0.7]Ga[sub 0.3]As Channel n-MOSFET with Self-Aligned Niâ€“InGaAs Source and Drain. Electrochemical and Solid-State Letters, 2011, 14, H60.	2.2	40
51	N-channel FinFETs With 25-nm Gate Length and Schottky-Barrier Source and Drain Featuring Ytterbium Silicide. IEEE Electron Device Letters, 2007, 28, 164-167.	2.2	39
52	High-mobility germanium-tin (GeSn) P-channel MOSFETs featuring metallic source/drain and sub-370 °C process modules. , 2011, , .		39
53	Strained n-Channel FinFETs Featuring In Situ Doped Siliconâ€“Carbon $(hbox{Si}_{1 - y}hbox{C}_{y})$ Source and Drain Stressors With High Carbon Content. IEEE Transactions on Electron Devices, 2008, 55, 2475-2483.	1.6	37
54	A new robust non-local algorithm for band-to-band tunneling simulation and its application to Tunnel-FET. Solid-State Electronics, 2011, 57, 23-30.	0.8	37

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55	Selenium Segregation for Effective Schottky Barrier Height Reduction in NiGe/nâ€“Ge Contacts. IEEE Electron Device Letters, 2012, 33, 773-775.	2.2	37
56	Enhanced performance in 50 nm N-MOSFETs with silicon-carbon source/drain regions. , 0, , .		36
57	In Situ Surface Passivation and CMOS-Compatible Palladiumâ€“Germanium Contacts for Surface-Channel Gallium Arsenide MOSFETs. IEEE Electron Device Letters, 2008, 29, 553-556.	2.2	36
58	Modeling Study of the Impact of Surface Roughness on Silicon and Germanium UTB MOSFETs. IEEE Transactions on Electron Devices, 2005, 52, 2430-2439.	1.6	35
59	Dopant Segregation and Nickel Stanogermanide Contact Formation on $hbox{p}^{+} hbox{Ge}_{0.947}hbox{Sn}_{0.053}$ Source/Drain. IEEE Electron Device Letters, 2012, 33, 634-636.	2.2	35
60	Ge0.83Sn0.17 p-channel metal-oxide-semiconductor field-effect transistors: Impact of sulfur passivation on gate stack quality. Journal of Applied Physics, 2016, 119, .	1.1	34
61	Above-bandgap optical properties of biaxially strained GeSn alloys grown by molecular beam epitaxy. Applied Physics Letters, 2014, 104, .	1.5	33
62	GeSn lateral p-i-n photodetector on insulating substrate. Optics Express, 2018, 26, 17312.	1.7	33
63	A Self-Aligned Ni-InGaAs Contact Technology for InGaAs Channel n-MOSFETs. Journal of the Electrochemical Society, 2012, 159, H511-H515.	1.3	32
64	GeSn-on-insulator substrate formed by direct wafer bonding. Applied Physics Letters, 2016, 109, .	1.5	31
65	Strained n-Channel Transistors With Silicon Source and Drain Regions and Embedded Silicon/Germanium as Strain-Transfer Structure. IEEE Electron Device Letters, 2007, 28, 609-612.	2.2	30
66	Strained germaniumâ€“tin (GeSn) p-channel metal-oxide-semiconductor field-effect-transistors (p-MOSFETs) with ammonium sulfide passivation. Solid-State Electronics, 2013, 83, 66-70.	0.8	30
67	Toward Conformal Damage-Free Doping With Abrupt Ultrashallow Junction: Formation of Si Monolayers and Laser Anneal as a Novel Doping Technique for InGaAs nMOSFETs. IEEE Transactions on Electron Devices, 2014, 61, 1039-1046.	1.6	30
68	Design and fabrication of 50-nm thin-body p-MOSFETs with a SiGe heterostructure channel. IEEE Transactions on Electron Devices, 2002, 49, 279-286.	1.6	29
69	Strained p-Channel FinFETs With Extended Pi-Shaped Siliconâ€“Germanium Source and Drain Stressors. IEEE Electron Device Letters, 2007, 28, 905-908.	2.2	29
70	Band alignment between amorphous Ge2Sb2Te5 and prevalent complementary-metal-oxide-semiconductor materials. Applied Physics Letters, 2008, 92, .	1.5	29
71	In-situ gallium-doping for forming p+ germanium-tin and application in germanium-tin p-i-n photodetector. Journal of Applied Physics, 2016, 119, .	1.1	29
72	Enhancement of memory window in short channel non-volatile memory devices using double layer tungsten nanocrystals. , 0, , .		28

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73	All-GaN Power Integration: Devices to Functional Subcircuits and Converter ICs. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2020, 8, 31-41.	3.7	28
74	Integrating GeSn photodiode on a 200 mm Ge-on-insulator photonics platform with Ge CMOS devices for advanced OEIC operating at 2 Î¼m band. Optics Express, 2019, 27, 26924.	1.7	28
75	I-MOS Transistor With an Elevated Siliconâ€“Germanium Impact-Ionization Region for Bandgap Engineering. IEEE Electron Device Letters, 2006, 27, 975-977.	2.2	27
76	Strained ${m n}$-MOSFET With Embedded Source/Drain Stressors and Strain-Transfer Structure (STS) for Enhanced Transistor Performance. IEEE Transactions on Electron Devices, 2008, 55, 850-857.	1.6	27
77	Dependence of the properties of phase change random access memory on nitrogen doping concentration in Ge2Sb2Te5. Journal of Applied Physics, 2010, 107, .	1.1	27
78	Performance Enhancement in Uniaxial Strained Silicon-on-Insulator N-MOSFETs Featuring Siliconâ€“Carbon Source/Drain Regions. IEEE Transactions on Electron Devices, 2007, 54, 2910-2917.	1.6	26
79	$hbox{Ni}(hbox{Ge}_{1 - x}hbox{Sn}_{x})$ Ohmic Contact Formation on N-Type $hbox{Ge}_{1 - x}hbox{Sn}_{x}$ Using Selenium or Sulfur Implant and Segregation. IEEE Transactions on Electron Devices, 2013, 60, 746-752.	1.6	26
80	Germanium-Tin (GeSn) P-Channel Fin Field-Effect Transistor Fabricated on a Novel GeSn-on-Insulator Substrate. IEEE Transactions on Electron Devices, 2018, 65, 3754-3761.	1.6	26
81	Compositional dependence of optical critical point parameters in pseudomorphic GeSn alloys. Journal of Applied Physics, 2014, 116, 053520.	1.1	25
82	Germanium-tin multiple quantum well on silicon avalanche photodiode for photodetection at two micron wavelength. Semiconductor Science and Technology, 2016, 31, 095001.	1.0	25
83	High-performance GeSn photodetector and fin field-effect transistor (FinFET) on an advanced GeSn-on-insulator platform. Optics Express, 2018, 26, 10305.	1.7	25
84	High-Permittivity Dielectric Stack on Gallium Nitride Formed by Silane Surface Passivation and Metalâ€“Organic Chemical Vapor Deposition. IEEE Electron Device Letters, 2010, 31, 8-10.	2.2	23
85	Strained germanium-tin (GeSn) N-channel MOSFETs featuring low temperature N+/P junction formation and GeSnO2 interfacial layer. , 2012, , .		23
86	Sub-400 Â°C Si₂H₆Passivation, HfO₂Gate Dielectric, and Single TaN Metal Gate: A Common Gate Stack Technology for In_{0.7}Ga_{0.3}As and Ge_{1-x}Sn_xCMOS. IEEE Transactions on Electron Devices, 2013, 60, 1640-1648.	1.6	23
87	Tunneling field-effect transistor with Ge/In0.53Ga0.47As heterostructure as tunneling junction. Journal of Applied Physics, 2013, 113, .	1.1	23
88	Ultra-low specific contact resistivity (1.4â€‰Ã—â€‰10â^'9 Î©Â·cm2) for metal contacts on in-situ Ga-doped Ge0.95Sn0.05 film. Journal of Applied Physics, 2017, 122, .	1.1	23
89	n-Channel GaAs MOSFET with TaNâ•HfAlO Gate Stack Formed Using In Situ Vacuum Anneal and Silane Passivation. Journal of the Electrochemical Society, 2008, 155, H464.	1.3	22
90	Crystal structure and epitaxial relationship of Ni4InGaAs2 films formed on InGaAs by annealing. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2013, 31, 012202.	0.6	22

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91	Germanium-based transistors for future high performance and low power logic applications. , 2015, , .		22
92	Performance enhancement of n-channel impact-ionization metal-oxide-semiconductor transistor by strain engineering. Applied Physics Letters, 2007, 90, 023505.	1.5	21
93	Enhanced Strain Effects in 25-nm Gate-Length Thin-Body nMOSFETs With Siliconâ€“Carbon Source/Drain and Tensile-Stress Liner. IEEE Electron Device Letters, 2007, 28, 301-304.	2.2	21
94	Silaneâ€“Ammonia Surface Passivation for Gallium Arsenide Surface-Channel n-MOSFETs. IEEE Electron Device Letters, 2009, 30, 110-112.	2.2	21
95	Superlatticelike dielectric as a thermal insulator for phase-change random access memory. Applied Physics Letters, 2010, 97, .	1.5	21
96	Au-Free AlGaN/GaN MIS-HEMTs With Embedded Current Sensing Structure for Power Switching Applications. IEEE Transactions on Electron Devices, 2017, 64, 3515-3518.	1.6	21
97	A new silane-ammonia surface passivation technology for realizing inversion-type surface-channel GaAs N-MOSFET with 160 nm gate length and high-quality metal-gate/high-k dielectric stack. , 2008, , .		20
98	Spacer Removal Technique for Boosting Strain in n-Channel FinFETs With Silicon-Carbon Source and Drain Stressors. IEEE Electron Device Letters, 2008, 29, 80-82.	2.2	20
99	SPICE Behavioral Model of the Tunneling Field-Effect Transistor for Circuit Simulation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 946-950.	2.2	20
100	Formation of epitaxial metastable NiGe2 thin film on Ge(100) by pulsed excimer laser anneal. Applied Physics Letters, 2010, 97, .	1.5	20
101	High-Performance Germanium $Omega$ -Gate MuGFET With Schottky-Barrier Nickel Germanide Source/Drain and Low-Temperature Disilane-Passivated Gate Stack. IEEE Electron Device Letters, 2012, 33, 1336-1338.	2.2	20
102	N-Channel (110)-Sidewall Strained FinFETs With Siliconâ€“Carbon Source and Drain Stressors and Tensile Capping Layer. IEEE Electron Device Letters, 2007, 28, 1014-1017.	2.2	19
103	Multiple-Gate In0.53Ga0.47As Channel n-MOSFETs with Self-Aligned Ni-InGaAs Contacts. ECS Journal of Solid State Science and Technology, 2012, 1, P82-P85.	0.9	19
104	Contact Resistance Reduction for Strained N-MOSFETs With Silicon-Carbon Source/Drain Utilizing Aluminum Ion Implant and Aluminum Profile Engineering. IEEE Transactions on Electron Devices, 2013, 60, 1310-1317.	1.6	19
105	A Double-Spacer I-MOS Transistor With Shallow Source Junction and Lightly Doped Drain for Reduced Operating Voltage and Enhanced Device Performance. IEEE Electron Device Letters, 2008, 29, 189-191.	2.2	18
106	Effective Modulation of Quadratic Voltage Coefficient of Capacitance in MIM Capacitors Using $hbox{Sm}_{2}hbox{O}_{3}/hbox{SiO}_{2}$ Dielectric Stack. IEEE Electron Device Letters, 2009, 30, 460-462.	2.2	18
107	Gate Stack Reliability of MOSFETs With High-Mobility Channel Materials: Bias Temperature Instability. IEEE Transactions on Device and Materials Reliability, 2013, 13, 524-533.	1.5	18
108	Self-assembly of tin wires via phase transformation of heteroepitaxial germanium-tin on germanium substrate. Journal of Applied Physics, 2015, 117, .	1.1	18

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109	The first GeSn FinFET on a novel GeSnOI substrate achieving lowest S of 79 mV/decade and record high Gm, int of 807 Î¼S/Î¼m for GeSn P-FETs. , 2017, , .		18
110	A High-Stress Liner Comprising Diamond-Like Carbon (DLC) for Strained p-Channel MOSFET. IEEE Electron Device Letters, 2008, 29, 192-194.	2.2	17
111	P-Channel Tri-Gate FinFETs Featuring $hbox{Ni}_{1 - y}hbox{Pt}_{y} hbox{SiGe}$ Source/Drain Contacts for Enhanced Drive Current Performance. IEEE Electron Device Letters, 2008, 29, 438-441.	2.2	17
112	Contact-Resistance Reduction for Strained n-FinFETs With Siliconâ€“Carbon Source/Drain and Platinum-Based Silicide Contacts Featuring Tellurium Implantation and Segregation. IEEE Transactions on Electron Devices, 2011, 58, 3852-3862.	1.6	17
113	Photoelectron spectroscopy study of band alignment at interface between Ni-InGaAs and In0.53Ga0.47As. Applied Physics Letters, 2011, 99, .	1.5	17
114	Self-Aligned Gate-First In[sub 0.7]Ga[sub 0.3]As n-MOSFETs with an InP Capping Layer for Performance Enhancement. Electrochemical and Solid-State Letters, 2011, 14, H117.	2.2	17
115	Germaniumâ€“Tin $hbox{n}^{+}hbox{/p}$ Junction Formed Using Phosphorus Ion Implant and 400 $^{circ} hbox{C}$ Rapid Thermal Anneal. IEEE Electron Device Letters, 2012, 33, 1529-1531.	2.2	17
116	Germanium n-Channel Planar FET and FinFET: Gate-Stack and Contact Optimization. IEEE Transactions on Electron Devices, 2015, 62, 3567-3574.	1.6	17
117	Carrier Transport Characteristics of Sub-30 nm Strained N-Channel FinFETs Featuring Silicon-Carbon Source/Drain Regions and Methods for Further Performance Enhancement. , 2006, , .		16
118	Full Silicidation of Silicon Gate Electrodes Using Nickel-Terbium Alloy for MOSFET Applications. Journal of the Electrochemical Society, 2006, 153, G337.	1.3	16
119	Pulsed Laser Annealing of Silicon-Carbon Source/Drain in MuGFETs for Enhanced Dopant Activation and High Substitutional Carbon Concentration. IEEE Electron Device Letters, 2008, 29, 464-467.	2.2	16
120	Digital Etch Technique for Forming Ultra-Scaled Germanium-Tin (Ge 1âˆ’x Sn x) Fin Structure. Scientific Reports, 2017, 7, 1835.	1.6	16
121	Source Engineering for Tunnel Field-Effect Transistor: Elevated Source with Vertical Siliconâ€“Germanium/Germanium Heterostructure. Japanese Journal of Applied Physics, 2011, 50, 04DJ07.	0.8	15
122	Simulation of tunneling field-effect transistors with extended source structures. Journal of Applied Physics, 2012, 111, 114514.	1.1	15
123	Ultimate Performance Projection of Ultrathin Body Transistor Based on Group IV, III-V, and 2-D-Materials. IEEE Transactions on Electron Devices, 2016, 63, 773-780.	1.6	15
124	Design of power integrated circuits in full AlGaN/GaN MISâ€HEMT configuration for power conversion. Physica Status Solidi (A) Applications and Materials Science, 2017, 214, 1600562.	0.8	15
125	Siliconâ€“Carbon Stressors With High Substitutional Carbon Concentration and In Situ Doping Formed in Source/Drain Extensions of n-Channel Transistors. IEEE Electron Device Letters, 2008, 29, 460-463.	2.2	14
126	Novel Nickel Silicide Contact Technology Using Selenium Segregation for SOI N-FETs With Siliconâ€“Carbon Source/Drain Stressors. IEEE Electron Device Letters, 2008, 29, 841-844.	2.2	14

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127	Achieving Conduction Band-Edge Schottky Barrier Height for Arsenic-Segregated Nickel Aluminide Disilicide and Implementation in FinFETs With Ultra-Narrow Fin Widths. IEEE Electron Device Letters, 2008, 29, 382-385.	2.2	14
128	Fermi-level depinning at the metal-germanium interface by the formation of epitaxial nickel digermanide NiGe2 using pulsed laser anneal. Applied Physics Letters, 2012, 101, .	1.5	14
129	Post-growth annealing of germanium-tin alloys using pulsed excimer laser. Journal of Applied Physics, 2015, 118, .	1.1	14
130	Heteroepitaxial growth of In0.30Ga0.70As high-electron mobility transistor on 200 mm silicon substrate using metamorphic graded buffer. AIP Advances, 2016, 6, 085106.	0.6	14
131	Sub <inline-formula> <tex-math notation="LaTeX">$10^{-extsf{9}},,Omegacdot{ext{cm}}^{extsf{2}}$ </tex-math> </inline-formula> Specific Contact Resistivity (Down to <inline-formula> <tex-math) Tj ETQq1 1 0.784314 rgBT /Overlock 10	1.6	14
132	Transactions on Electron Devices, 2018, 65, 5275-5281. Novel Nickel-Alloy Silicides for Source/Drain Contact Resistance Reduction in N-Channel Multiple-Gate Transistors with Sub-35nm Gate Length. , 2006, , .		13
133	Strained Thin-Body p-MOSFET With Condensed Silicon-Germanium Source/Drain for Enhanced Drive Current Performance. IEEE Electron Device Letters, 2007, 28, 509-512.	2.2	13
134	Work Function Tunability of Refractory Metal Nitrides by Lanthanum or Aluminum Doping for Advanced CMOS Devices. IEEE Transactions on Electron Devices, 2007, 54, 2871-2877.	1.6	13
135	Fabrication of p-MOSFETs on Germanium Epitaxially Grown on Gallium Arsenide Substrate by Chemical Vapor Deposition. Journal of the Electrochemical Society, 2008, 155, H76.	1.3	13
136	Modeling the Negative Quadratic VCC of $hbox{SiO}_{2}$ in MIM Capacitor. IEEE Electron Device Letters, 2011, 32, 1671-1673.	2.2	13
137	Contact Technology for Strained nFinFETs With Siliconâ€“Carbon Source/Drain Stressors Featuring Sulfur Implant and Segregation. IEEE Transactions on Electron Devices, 2012, 59, 1046-1055.	1.6	13
138	Influence of hydrogen surface passivation on Sn segregation, aggregation, and distribution in GeSn/Ge(001) materials. Journal of Applied Physics, 2015, 117, .	1.1	13
139	Development of GaN Power IC Platform and All GaN DC-DC Buck Converter IC. , 2019, , .		13
140	CoInGaAs as a novel self-aligned metallic source/drain material for implant-less In0.53Ga0.47As n-MOSFETs. Solid-State Electronics, 2012, 78, 62-67.	0.8	12
141	Germanium Multiple-Gate Field-Effect Transistor With In Situ Boron-Doped Raised Source/Drain. IEEE Transactions on Electron Devices, 2013, 60, 2135-2141.	1.6	12
142	Towards simultaneous achievement of carrier activation and crystallinity in Ge and GeSn with heated phosphorus ion implantation: An optical study. Applied Physics Letters, 2014, 105, 122108.	1.5	12
143	Band alignment of HfO2/Al0.25Ga0.75N determined by x-ray photoelectron spectroscopy: Effect of SiH4 surface treatment. Applied Physics Letters, 2014, 104, 091605.	1.5	12
144	Silicon Surface Passivation Technology for Germanium-Tin P-Channel MOSFETs: Suppression of Germanium and Tin Segregation for Mobility Enhancement. ECS Journal of Solid State Science and Technology, 2014, 3, Q162-Q168.	0.9	12

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145	Gate-All-Around In_{0.53}Ga_{0.47}As Junctionless Nanowire FET With Tapered Source/Drain Structure. IEEE Transactions on Electron Devices, 2016, 63, 1027-1033.	1.6	12
146	Thin body silicon-on-insulator N-MOSFET with silicon-carbon source/drain regions for performance enhancement. , 0, , .		11
147	Thermally robust TaTb/sub x/N metal gate electrode for n-MOSFETs applications. IEEE Electron Device Letters, 2005, 26, 75-77.	2.2	11
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