Chenming Hu

List of Publications by Year
in descending order

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393 papers	20,672 citations	18436 62 h-index	16605 123 g-index
397 all docs	397 docs citations	397 times ranked	10733 citing authors

#	Article	IF	Citations
1	Robust Compact Model of High-Voltage MOSFETâ€™s Drift Region. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 337-340.	1.9	8
2	A Compact Model of Antiferroelectric Capacitor. IEEE Electron Device Letters, 2022, 43, 316-318.	2.2	3
3	A Compact Model of Metalâ€“Ferroelectric-Insulatorâ€“Semiconductor Tunnel Junction. IEEE Transactions on Electron Devices, 2022, 69, 414-418.	1.6	6
4	Enhancement of Ferroelectricity in 5 nm Metal-Ferroelectric-Insulator Technologies by Using a Strained TiN Electrode. Nanomaterials, 2022, 12, 468.	1.9	2
5	Engineering Hf_{0.5}Zr_{0.5}O₂ Ferroelectric/Anti- Ferroelectric Phases With Oxygen Vacancy and Interface Energy Achieving High Remanent Polarization and Dielectric Constants. IEEE Electron Device Letters, 2022, 43, 553-556.	2.2	19
6	Fast Read-After-Write and Depolarization Fields in High Endurance n-Type Ferroelectric FETs. IEEE Electron Device Letters, 2022, 43, 717-720.	2.2	23
7	Ultrathin ferroic HfO2â€“ZrO2 superlattice gate stack for advanced transistors. Nature, 2022, 604, 65-71.	13.7	108
8	Deep-Learning-Assisted Physics-Driven MOSFET Current-Voltage Modeling. IEEE Electron Device Letters, 2022, 43, 974-977.	2.2	32
9	van der Waals epitaxy of 2D h-AlN on TMDs by atomic layer deposition at 250â€‰Â°C. Applied Physics Letters, 2022, 120, .	1.5	13
10	A Compact Model of Nanoscale Ferroelectric Capacitor. IEEE Transactions on Electron Devices, 2022, 69, 4761-4764.	1.6	1
11	A Compact Model of Ferroelectric Field-Effect Transistor. IEEE Electron Device Letters, 2022, 43, 1363-1366.	2.2	5
12	Deep Learning-Based BSIM-CMG Parameter Extraction for 10-nm FinFET. IEEE Transactions on Electron Devices, 2022, 69, 4765-4768.	1.6	17
13	Electric Field-Induced Permittivity Enhancement in Negative-Capacitance FET. IEEE Transactions on Electron Devices, 2021, 68, 1346-1351.	1.6	10
14	Energy Storage and Reuse in Negative Capacitance. IEEE Transactions on Electron Devices, 2021, 68, 1861-1865.	1.6	2
15	Compact Modeling of Temperature Effects in FDSOI and FinFET Devices Down to Cryogenic Temperatures. IEEE Transactions on Electron Devices, 2021, 68, 4223-4230.	1.6	38
16	S-Curve Engineering for ON-State Performance Using Anti-Ferroelectric/Ferroelectric Stack Negative-Capacitance FinFET. IEEE Transactions on Electron Devices, 2021, 68, 4787-4792.	1.6	4
17	Single-Crystal Islands (SCI) for Monolithic 3-D and Back-End-of-Line FinFET Circuits. IEEE Transactions on Electron Devices, 2021, 68, 5257-5262.	1.6	4
18	A Compact Model of Polycrystalline Ferroelectric Capacitor. IEEE Transactions on Electron Devices, 2021, 68, 5311-5314.	1.6	15

#	Article	IF	Citations
19	Ferroelectric HfO₂ Memory Transistors With High-Î² Interfacial Layer and Write Endurance Exceeding 10¹⁰ Cycles. IEEE Electron Device Letters, 2021, 42, 994-997.	2.2	117
20	Near Threshold Capacitance Matching in a Negative Capacitance FET With 1 nm Effective Oxide Thickness Gate Stack. IEEE Electron Device Letters, 2020, 41, 179-182.	2.2	30
21	BSIM Compact Model of Quantum Confinement in Advanced Nanosheet FETs. IEEE Transactions on Electron Devices, 2020, 67, 730-737.	1.6	38
22	Experimental Demonstration of a Ferroelectric HfO₂-Based Content Addressable Memory Cell. IEEE Electron Device Letters, 2020, 41, 240-243.	2.2	45
23	Highly Scaled, High Endurance, Î©-Gate, Nanowire Ferroelectric FET Memory Transistors. IEEE Electron Device Letters, 2020, 41, 1637-1640.	2.2	39
24	Reliability of Ferroelectric HfO₂-based Memories: From MOS Capacitor to FeFET. , 2020, , .		6
25	Modeling of Current Mismatch and 1/f Noise for Halo-Implanted Drain-Extended MOSFETs. IEEE Transactions on Electron Devices, 2020, 67, 4794-4801.	1.6	4
26	Design Optimization Techniques in Nanosheet Transistor for RF Applications. IEEE Transactions on Electron Devices, 2020, 67, 4515-4520.	1.6	26
27	Analysis and Modeling of Polarization Gradient Effect on Negative Capacitance FET. IEEE Transactions on Electron Devices, 2020, 67, 4521-4525.	1.6	13
28	Gate-All-Around FET Design Rule for Suppression of Excess Non-Linearity. IEEE Electron Device Letters, 2020, 41, 1750-1753.	2.2	4
29	Improved TDDB Reliability and Interface States in 5-nm Hf_{0.5}Zr_{0.5}O₂ Ferroelectric Technologies Using NH₃ Plasma and Microwave Annealing. IEEE Transactions on Electron Devices, 2020, 67, 1581-1585.	1.6	32
30	A New 8T Hybrid Nonvolatile SRAM With Ferroelectric FET. IEEE Journal of the Electron Devices Society, 2020, 8, 171-175.	1.2	19
31	Compact Model for Geometry Dependent Mobility in Nanosheet FETs. IEEE Electron Device Letters, 2020, 41, 313-316.	2.2	22
32	Optimization of Negative-Capacitance Vertical-Tunnel FET (NCVT-FET). IEEE Transactions on Electron Devices, 2020, 67, 2593-2599.	1.6	53
33	Enhanced ferroelectricity in ultrathin films grown directly on silicon. Nature, 2020, 580, 478-482.	13.7	486
34	Accurate and Computationally Efficient Modeling of Nonquasi Static Effects in MOSFETs for Millimeter-Wave Applications. IEEE Transactions on Electron Devices, 2019, 66, 44-51.	1.6	13
35	Anomalously Beneficial Gate-Length Scaling Trend of Negative Capacitance Transistors. IEEE Electron Device Letters, 2019, 40, 1860-1863.	2.2	16
36	Challenges to Partial Switching of Hf_{0.8}Zr_{0.2}O₂ Gated Ferroelectric FET for Multilevel/Analog or Low-Voltage Memory Operation. IEEE Electron Device Letters, 2019, 40, 1423-1426.	2.2	27

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37	Ferroelectric Si-doped HfO2 Capacitors for Next-Generation Memories. , 2019, , .		1
38	Effects of Annealing on Ferroelectric Hafniumâ€“Zirconiumâ€“Oxide-Based Transistor Technology. IEEE Electron Device Letters, 2019, 40, 467-470.	2.2	25
39	Improved Modeling of Bulk Charge Effect for BSIM-BULK Model. IEEE Transactions on Electron Devices, 2019, 66, 2850-2853.	1.6	8
40	Characterization and Modeling of Flicker Noise in FinFETs at Advanced Technology Node. IEEE Electron Device Letters, 2019, 40, 985-988.	2.2	28
41	Spacer Engineering in Negative Capacitance FinFETs. IEEE Electron Device Letters, 2019, 40, 1009-1012.	2.2	36
42	Negative Capacitance FET With 1.8-nm-Thick Zr-Doped HfO₂ Oxide. IEEE Electron Device Letters, 2019, 40, 993-996.	2.2	106
43	Optimization of NCFET by Matching Dielectric and Ferroelectric Nonuniformly Along the Channel. IEEE Electron Device Letters, 2019, 40, 822-825.	2.2	16
44	Evaluation of NC-FinFET Based Subsystem-Level Logic Circuits. IEEE Transactions on Electron Devices, 2019, 66, 2004-2009.	1.6	28
45	Analysis and Modeling of Inner Fringing Field Effect on Negative Capacitance FinFETs. IEEE Transactions on Electron Devices, 2019, 66, 2023-2027.	1.6	37
46	Monolithic 3D BEOL FinFET switch arrays using location-controlled-grain technique in voltage regulator with better FOM than 2D regulators. , 2019, , .		16
47	Proposal for Capacitance Matching in Negative Capacitance Field-Effect Transistors. IEEE Electron Device Letters, 2019, 40, 463-466.	2.2	66
48	Spatially resolved steady-state negative capacitance. Nature, 2019, 565, 468-471.	13.7	245
49	Compact Modeling of Cross-Sectional Scaling in Gate-All-Around FETs: 3-D to 1-D Transition. IEEE Transactions on Electron Devices, 2018, 65, 1094-1100.	1.6	18
50	Designing 0.5 V 5-nm HP and 0.23 V 5-nm LP NC-FinFETs With Improved ${I}_{ mathrm{scriptscriptstyle OFF}}$ Sensitivity in Presence of Parasitic Capacitance. IEEE Transactions on Electron Devices, 2018, 65, 1211-1216.	1.6	31
51	Engineering Negative Differential Resistance in NCFETs for Analog Applications. IEEE Transactions on Electron Devices, 2018, 65, 2033-2039.	1.6	79
52	Improved Subthreshold Swing and Short Channel Effect in FDSOI n-Channel Negative Capacitance Field Effect Transistors. IEEE Electron Device Letters, 2018, 39, 300-303.	2.2	128
53	A Nitrided Interfacial Oxide for Interface State Improvement in Hafnium Zirconium Oxide-Based Ferroelectric Transistor Technology. IEEE Electron Device Letters, 2018, 39, 95-98.	2.2	24
54	Evaluation of NC-FinFET Based Subsystem-Level Logic Circuits Using SPICE Simulation. , 2018, , .		3

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55	Location-controlled-grain Technique for Monolithic 3D BEOL FinFET Circuits. , 2018, , .		16
56	Negative-Capacitance FinFET Inverter, Ring Oscillator, SRAM Cell, and Ft. , 2018, , .		19
57	Response Speed of Negative Capacitance FinFETs. , 2018, , .		29
58	Negative Capacitance, n-Channel, Si FinFETs: Bi-directional Sub-60 mV/dec, Negative DIBL, Negative Differential Resistance and Improved Short Channel Effect. , 2018, , .		43
59	A Unified Flicker Noise Model for FDSOI MOSFETs Including Back-bias Effect. , 2018, , .		7
60	Variation Caused by Spatial Distribution of Dielectric and Ferroelectric Grains in a Negative Capacitance Field-Effect Transistor. IEEE Transactions on Electron Devices, 2018, 65, 4652-4658.	1.6	29
61	UTBSOI MOSFET with corner spacers for energy-efficient applications. , 2018, , .		3
62	Modeling of Induced Gate Thermal Noise Including Back-Bias Effect in FDSOI MOSFET. IEEE Microwave and Wireless Components Letters, 2018, 28, 597-599.	2.0	6
63	NCFET Design Considering Maximum Interface Electric Field. IEEE Electron Device Letters, 2018, 39, 1254-1257.	2.2	33
64	Analysis and Modeling of Temperature and Bias Dependence of Current Mismatch in Halo-Implanted MOSFETs. IEEE Transactions on Electron Devices, 2018, 65, 3608-3616.	1.6	12
65	Anomalous Transconductance in Long Channel Halo Implanted MOSFETs: Analysis and Modeling. IEEE Transactions on Electron Devices, 2017, 64, 376-383.	1.6	15
66	A Predictive Tunnel FET Compact Model With Atomistic Simulation Validation. IEEE Transactions on Electron Devices, 2017, 64, 599-605.	1.6	20
67	Bulk FinFET With Low- $kappa $ Spacers for Continued Scaling. IEEE Transactions on Electron Devices, 2017, 64, 1861-1864.	1.6	38
68	Investigation of Mo/Ti/AlN/HfO2High-k Metal Gate Stack for Low Power Consumption InGaAs NMOS Device Application. IEEE Electron Device Letters, 2017, 38, 552-555.	2.2	9
69	Modeling of Body-Bias Dependence of Overlap Capacitances in Bulk MOSFETs. , 2017, , .		1
70	Compact Modeling of Drain Current Thermal Noise in FDSOI MOSFETs Including Back-Bias Effect. IEEE Transactions on Microwave Theory and Techniques, 2017, 65, 2261-2270.	2.9	14
71	Self-Aligned, Gate Last, FDSOI, Ferroelectric Gate Memory Device With 5.5-nm Hf_{0.8}Zr_{0.2}O₂, High Endurance and Breakdown Recovery. IEEE Electron Device Letters, 2017, 38, 1379-1382.	2.2	76
72	Compact Modeling Source-to-Drain Tunneling in Sub-10-nm GAA FinFET With Industry Standard Model. IEEE Transactions on Electron Devices, 2017, 64, 3576-3581.	1.6	13

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73	High V<inf>th</inf> enhancement mode GaN power devices with high I<inf>D, max</inf> using hybrid ferroelectric charge trap gate stack. , 2017, , .		4
74	Modeling of Back-Gate Effects on Gate-Induced Drain Leakage and Gate Currents in UTB SOI MOSFETs. IEEE Transactions on Electron Devices, 2017, 64, 3986-3990.	1.6	9
75	Stabilization of ferroelectric phase in tungsten capped Hf0.8Zr0.2O2. Applied Physics Letters, 2017, 111, .	1.5	58
76	High-gain monolithic 3D CMOS inverter using layered semiconductors. Applied Physics Letters, 2017, 111, .	1.5	8
77	Nanowire FET With Corner Spacer for High-Performance, Energy-Efficient Applications. IEEE Transactions on Electron Devices, 2017, 64, 5181-5187.	1.6	23
78	Stressor design for FinFETs with air-gap spacers. , 2017, , .		0
79	Ferroelectricity in HfO<inf>2</inf> thin films as a function of Zr doping. , 2017, , .		5
80	FinFET With Encased Air-Gap Spacers for High-Performance and Low-Energy Circuits. IEEE Electron Device Letters, 2017, 38, 16-19.	2.2	42
81	Impact of Parasitic Capacitance and Ferroelectric Parameters on Negative Capacitance FinFET Characteristics. IEEE Electron Device Letters, 2017, 38, 142-144.	2.2	71
82	Differential voltage amplification from ferroelectric negative capacitance. Applied Physics Letters, 2017, 111, .	1.5	36
83	Impact of Al content on InAs/AlSb/Al _x Ga _{1â^' x} Sb tunnelling diode. Journal of Engineering, 2017, 2017, 403-406.	0.6	0
84	Compact models of negative-capacitance FinFETs: Lumped and distributed charge models. , 2016, , .		69
85	Modeling of Subsurface Leakage Current in Low Short Channel MOSFET at Accumulation Bias. IEEE Transactions on Electron Devices, 2016, 63, 1840-1845.	1.6	14
86	MoS ₂ transistors with 1-nanometer gate lengths. Science, 2016, 354, 99-102.	6.0	1,140
87	Corner spacer design for performance optimization of multi-gate InGaAs-OI FinFET with gate-to-source/drain underlap. , 2016, , .		6
88	Modeling of Charge and Quantum Capacitance in Low Effective Mass III-V FinFETs. IEEE Journal of the Electron Devices Society, 2016, 4, 396-401.	1.2	13
89	Study of Inherent Gate Coupling Nonuniformity of InAs/GaSb Vertical TFETs. IEEE Transactions on Electron Devices, 2016, 63, 4267-4272.	1.6	8
90	Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistanceâ€"Part I: Model Description. IEEE Transactions on Electron Devices, 2016, 63, 4981-4985.	1.6	85

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91	Methods for Extracting Flat Band Voltage in the InGaAs High Mobility Materials. IEEE Electron Device Letters, 2016, 37, 1100-1103.	2.2	7
92	Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistanceâ€"Part II: Model Validation. IEEE Transactions on Electron Devices, 2016, 63, 4986-4992.	1.6	139
93	Modeling of threshold voltage for operating point using industry standard BSIM-IMG model. , 2016, , .		6
94	FinFET With High-<inline-formula> <tex-math notation="LaTeX">$kappa $ </tex-math> </inline-formula> Spacers for Improved Drive Current. IEEE Electron Device Letters, 2016, 37, 835-838.	2.2	52
95	RF Modeling of FDSOI Transistors Using Industry Standard BSIM-IMG Model. IEEE Transactions on Microwave Theory and Techniques, 2016, 64, 1745-1751.	2.9	34
96	Monolithic 3D CMOS Using Layered Semiconductors. Advanced Materials, 2016, 28, 2547-2554.	11.1	107
97	Effects of the Variation of Ferroelectric Properties on Negative Capacitance FET Characteristics. IEEE Transactions on Electron Devices, 2016, 63, 2197-2199.	1.6	160
98	Single crystal functional oxides on silicon. Nature Communications, 2016, 7, 10547.	5.8	156
99	Suppressing Non-Uniform Tunneling in InAs/GaSb TFET With Dual-Metal Gate. IEEE Journal of the Electron Devices Society, 2016, 4, 60-65.	1.2	22
100	Negative Capacitance in Short-Channel FinFETs Externally Connected to an Epitaxial Ferroelectric Capacitor. IEEE Electron Device Letters, 2016, 37, 111-114.	2.2	198
101	2D layered materials: From materials properties to device applications. , 2015, , .		9
102	Analytical Modeling of Flicker Noise in Halo Implanted MOSFETs. IEEE Journal of the Electron Devices Society, 2015, 3, 355-360.	1.2	22
103	Modeling SiGe FinFETs With Thin Fin and Current-Dependent Source/Drain Resistance. IEEE Electron Device Letters, 2015, 36, 636-638.	2.2	7
104	Electrostatic integrity and performance enhancement for UTB InGaAs-OI MOSFET with high-k dielectric through spacer design. , 2015, , .		3
105	Sub-60mV-swing negative-capacitance FinFET without hysteresis. , 2015, , .		163
106	Analytical Modeling and Experimental Validation of Threshold Voltage in BSIM6 MOSFET Model. IEEE Journal of the Electron Devices Society, 2015, 3, 240-243.	1.2	22
107	BSIM-CMG: Standard FinFET compact model for advanced circuit design. , 2015, , .		65
108	Quantum Well InAs/AlSb/GaSb Vertical Tunnel FET With HSQ Mechanical Support. IEEE Nanotechnology Magazine, 2015, 14, 580-584.	1.1	19

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109	Modeling STI Edge Parasitic Current for Accurate Circuit Simulations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1291-1294.	1.9	11
110	BSIM-IMG: Compact model for RF-SOI MOSFETs. , 2015, , .		13
111	Piezoelectricity-Induced Schottky Barrier Height Variations in AlGaN/GaN High Electron Mobility Transistors. IEEE Electron Device Letters, 2015, 36, 902-904.	2.2	27
112	New industry standard FinFET compact model for future technology nodes. , 2015, , .		12
113	Capacitance Modeling in IIIâ€“V FinFETs. IEEE Transactions on Electron Devices, 2015, 62, 3892-3897.	1.6	25
114	Hybrid Si/TMD 2D electronic double channels fabricated using solid CVD few-layer-MoS2 stacking for V<inf>th</inf> matching and CMOS-compatible 3DFETs. , 2014, , .		12
115	Modeling 20-nm Germanium FinFET With the Industry Standard FinFET Model. IEEE Electron Device Letters, 2014, 35, 711-713.	2.2	20
116	Series resistance and mobility in mechanically-exfoliated layered transition metal dichalcogenide MOSFETs. , 2014, , .		2
117	Impact of channel doping on the device and NBTI performance in FinFETs for low power applications. , 2014, , .		1
118	Modeling of GaN-Based Normally-Off FinFET. IEEE Electron Device Letters, 2014, 35, 612-614.	2.2	40
119	BSIM-IMG with improved surface potential calculation recipe. , 2014, , .		5
120	Two-dimensional to three-dimensional tunneling in InAs/AlSb/GaSb quantum well heterojunctions. Journal of Applied Physics, 2013, 114, .	1.1	16
121	High sensitivity DNA sieving technology by entropic trapping in 3D artificial nano-channel matrices. , 2013, , .		1
122	Unified FinFET compact model: Modelling Trapezoidal Triple-Gate FinFETs. , 2013, , .		28
123	Monolithic 3D chip integrated with 500ns NVM, 3ps logic circuits and SRAM. , 2013, , .		32
124	Compact modeling for the changing transistor. , 2013, , .		2
125	Low power negative capacitance FETs for future quantum-well body technology. , 2013, , .		19
126	Device design considerations for ultra-thin body non-hysteretic negative capacitance FETs. , 2013, , .		24

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127	Interfacial layer reduction and high permittivity tetragonal ZrO2 on germanium reaching ultrathin 0.39â€‰nm equivalent oxide thickness. Applied Physics Letters, 2013, 102, .	1.5	16
128	Record-high 121/62 μA/μm on-currents 3D stacked epi-like Si FETs with and without metal back gate. , 2013, , .		21
129	Threshold Vacuum Switch (TVS) on 3D-stackable and 4F² cross-point bipolar and unipolar resistive random access memory. , 2012, , .		4
130	3D Ferroelectric-like NVM/CMOS hybrid chip by sub-400 °C sequential layered integration. , 2012, , .		5
131	A little known benefit of FinFET over Planar MOSFET in highperformance circuits at advanced technology nodes. , 2012, , .		9
132	A non-iterative physical procedure for RF CMOS compact model extraction using BSIM6. , 2012, , .		9
133	Hybrid CIS/Si near-IR sensor and 16% PV energy-harvesting technology. , 2012, , .		0
134	Fast programming metal-gate Si quantum dot nonvolatile memory using green nanosecond laser spike annealing. Applied Physics Letters, 2012, 100, .	1.5	40
135	Random Telegraph Noise in 1X-nm CMOS Silicide Contacts and a Method to Extract Trap Density. IEEE Electron Device Letters, 2012, 33, 591-593.	2.2	1
136	Denser and More Stable SRAM Using FinFETs With Multiple Fin Heights. IEEE Transactions on Electron Devices, 2012, 59, 2037-2041.	1.6	42
137	Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation. , 2011, , .		241
138	User verify and disturb mechanisms in a 65nm flash FPGA. , 2011, , .		0
139	BSIM-CG: A compact model of cylindrical gate / nanowire MOSFETs for circuit simulations. , 2011, , .		1
140	Modeling intrinsic and extrinsic asymmetry of 3D cylindrical gate/gate-all-around FETs for circuit simulations. , 2011, , .		4
141	Denser and more stable FinFET SRAM using multiple fin heights. , 2011, , .		1
142	A Novel Nanoinjection Lithography (NInL) Technology and Its Application for 16-nm Node Device Fabrication. IEEE Transactions on Electron Devices, 2011, 58, 3678-3686.	1.6	5
143	A novel bottom-up Ag contact (30nm diameter and 6.5 aspect ratio) technology by electroplating for 1Xnm and beyond technology. , 2011, , .		0
144	Bifacial CIGS (11% efficiency)/Si solar cells by Cd-free and sodium-free green process integrated with CIGS TFTs. , 2011, , .		5

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145	Silicide barrier engineering induced random telegraph noise in 1Xnm CMOS contacts. , 2011, , .		0
146	Ultrathin body InAs tunneling field-effect transistors on Si substrates. Applied Physics Letters, 2011, 98, .	1.5	76
147	Novel 140°C hybrid thin film solar cell/transistor technology with 9.6% conversion efficiency and 1.1 cm²/V-s electron mobility for low-temperature substrates. , 2010, , .		3
148	The effects of vacuum spacer transistors between high performance and low stand-by power devices beyond 16nm. , 2010, , .		1
149	Tunnel Field Effect Transistor With Raised Germanium Source. IEEE Electron Device Letters, 2010, 31, 1107-1109.	2.2	141
150	Global parameter extraction for a multi-gate MOSFETs compact model. , 2010, , .		15
151	Prospect of tunneling green transistor for 0.1V CMOS. , 2010, , .		61
152	Cycling induced degradation of a 65nm FPGA flash memory switch. , 2010, , .		2
153	16nm functional 0.039µm² 6T-SRAM cell with nano injection lithography, nanowire channel, and full TiN gate. , 2009, , .		5
154	Air-Spacer MOSFET With Self-Aligned Contact for Future Dense Memories. IEEE Electron Device Letters, 2009, 30, 1368-1370.	2.2	19
155	A comprehensive study of Ge<inf>1−x</inf>Si<inf>x</inf> on Ge for the Ge nMOSFETs with tensile stress, shallow junctions and reduced leakage. , 2009, , .		4
156	Design of FinFET SRAM Cells Using a Statistical Compact Model. , 2009, , .		15
157	A Low Voltage Steep Turn-Off Tunnel Transistor Design. , 2009, , .		19
158	Gate last MOSFET with air spacer and self-aligned contacts for dense memories. , 2009, , .		2
159	Flicker-Noise Impact on Scaling of Mixed-Signal CMOS With HfSiON. IEEE Transactions on Electron Devices, 2008, 55, 417-422.	1.6	9
160	Feedback FET: A novel transistor exhibiting steep switching behavior at low bias voltages. , 2008, , .		72
161	Green transistor as a solution to the IC power crisis. , 2008, , .		41
162	Green Transistor - A V<inf>DD</inf> Scaling Path for Future Low Power ICs. International Power Modulator Symposium and High-Voltage Workshop, 2008, , .	0.0	26

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163	Air spacer MOSFET technology for 20nm node and beyond. , 2008, , .		6
164	Statistical Compact Modeling of Variations in Nano MOSFETs. , 2008, , .		10
165	Low-voltage green transistor using hetero-tunneling. , 2008, , .		3
166	Low-voltage green transistor using ultra shallow junction and hetero-tunneling. , 2008, , .		18
167	Air-spacer Self-Aligned Contact MOSFET for future dense memories. , 2008, , .		0
168	Effect of Top Electrode Material on Resistive Switching Properties of $hbox{ZrO}_{2}$ Film Memory Devices. IEEE Electron Device Letters, 2007, 28, 366-368.	2.2	302
169	Modified resistive switching behavior of ZrO2 memory films based on the interface layer formed by using Ti top electrode. Journal of Applied Physics, 2007, 102, 094101.	1.1	131
170	Random telegraph noise in flash memories - model and technology scaling. , 2007, , .		95
171	A Multi-Gate MOSFET Compact Model Featuring Independent-Gate Operation. , 2007, , .		21
172	BSIM-MG: A Versatile Multi-Gate FET Model for Mixed-Signal Design. , 2007, , .		37
173	MOSFET hot-carrier reliability improvement by forward-body bias. IEEE Electron Device Letters, 2006, 27, 605-608.	2.2	29
174	Effect of Fluorine Incorporation on 1/f Noise of HfSiON FETs for Future Mixed-Signal CMOS. , 2006, , .		11
175	MOSFET design for forward body biasing scheme. IEEE Electron Device Letters, 2006, 27, 387-389.	2.2	38
176	Bias Polarity Dependent Effects of>tex<$rm P+$>/tex<Floating Gate EEPROMs. IEEE Transactions on Electron Devices, 2004, 51, 282-285.	1.6	9
177	Characterization of Spatial Intrafield Gate CD Variability, Its Impact on Circuit Performance, and Spatial Mask-Level Correction. IEEE Transactions on Semiconductor Manufacturing, 2004, 17, 2-11.	1.4	75
178	MOSFET gate leakage modeling and selection guide for alternative gate dielectrics based on leakage considerations. IEEE Transactions on Electron Devices, 2003, 50, 1027-1035.	1.6	192
179	Loop-based interconnect modeling and optimization approach for multigigahertz clock network design. IEEE Journal of Solid-State Circuits, 2003, 38, 457-463.	3.5	27
180	Improved a priori interconnect predictions and technology extrapolation in the GTX system. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2003, 11, 3-14.	2.1	10

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181	Frequency-independent equivalent-circuit model for on-chip spiral inductors. IEEE Journal of Solid-State Circuits, 2003, 38, 419-426.	3.5	306
182	RF characterization of metal T-gate structure in fully-depleted SOI CMOS technology. IEEE Electron Device Letters, 2003, 24, 251-253.	2.2	9
183	On the body-source built-in potential lowering of SOI MOSFETs. IEEE Electron Device Letters, 2003, 24, 90-92.	2.2	12
184	Direct tunneling RAM (DT-RAM) for high-density memory applications. IEEE Electron Device Letters, 2003, 24, 475-477.	2.2	2
185	Dual work function metal gate CMOS transistors by Ni-Ti interdiffusion. IEEE Electron Device Letters, 2002, 23, 200-202.	2.2	79
186	Direct tunneling leakage current and scalability of alternative gate dielectrics. Applied Physics Letters, 2002, 81, 2091-2093.	1.5	184
187	JVD silicon nitride as tunnel dielectric in p-channel flash memory. IEEE Electron Device Letters, 2002, 23, 91-93.	2.2	20
188	Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology. Journal of Applied Physics, 2002, 92, 7266-7271.	1.1	393
189	A thermal activation view of low voltage impact ionization in MOSFETs. IEEE Electron Device Letters, 2002, 23, 550-552.	2.2	31
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