Chenming Hu

List of Publications by Year in Descending Order

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

345 papers	14,645 citations	57 h-index	112 g-index
397 ext. papers	17,385 ext. citations	4.2 avg, IF	6.32 L-index

#	Paper	IF	Citations
345	A Compact Model of Metal□Ferroelectric-Insulator□Semiconductor Tunnel Junction. *IEEE Transactions on Electron Devices*, **2022**, 69, 414-418	2.9	2
344	Engineering Hf0.5Zr0.5O2 Ferroelectric/Anti-ferroelectric Phases with Oxygen Vacancy and Interface Energy Achieving High Remanent Polarization and Dielectric Constants. *IEEE Electron Device Letters*, **2022**, 1-1	4.4	5
343	Fast Read-After-Write and Depolarization Fields in High Endurance n-Type Ferroelectric FETs. *IEEE Electron Device Letters*, **2022**, 1-1	4.4	6
342	Ultrathin ferroic HfO-ZrO superlattice gate stack for advanced transistors.. *Nature*, **2022**, 604, 65-71	50.4	13
341	Deep-Learning-Assisted Physics-Driven MOSFET Current-Voltage Modeling. *IEEE Electron Device Letters*, **2022**, 1-1	4.4	2
340	van der Waals epitaxy of 2D h-AlN on TMDs by atomic layer deposition at 250 □C. *Applied Physics Letters*, **2022**, 120, 162102	3.4	1
339	Robust Compact Model of High Voltage MOSFET□ Drift Region. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2022**, 1-1	2.5	1
338	A Compact Model of Antiferroelectric Capacitor. *IEEE Electron Device Letters*, **2021**, 1-1	4.4	1
337	Electric Field-Induced Permittivity Enhancement in Negative-Capacitance FET. *IEEE Transactions on Electron Devices*, **2021**, 68, 1346-1351	2.9	4
336	Energy Storage and Reuse in Negative Capacitance. *IEEE Transactions on Electron Devices*, **2021**, 68, 1861-1865	2.9	0
335	Compact Modeling of Temperature Effects in FDSOI and FinFET Devices Down to Cryogenic Temperatures. *IEEE Transactions on Electron Devices*, **2021**, 68, 4223-4230	2.9	6
334	S-Curve Engineering for ON-State Performance Using Anti-Ferroelectric/Ferroelectric Stack Negative-Capacitance FinFET. *IEEE Transactions on Electron Devices*, **2021**, 68, 4787-4792	2.9	1
333	Single-Crystal Islands (SCI) for Monolithic 3-D and Back-End-of-Line FinFET Circuits. *IEEE Transactions on Electron Devices*, **2021**, 68, 5257-5262	2.9	0
332	A Compact Model of Polycrystalline Ferroelectric Capacitor. *IEEE Transactions on Electron Devices*, **2021**, 68, 5311-5314	2.9	6
331	Ferroelectric HfO2 Memory Transistors With High-□Interfacial Layer and Write Endurance Exceeding 1010 Cycles. *IEEE Electron Device Letters*, **2021**, 1-1	4.4	49
330	Gate-All-Around FET Design Rule for Suppression of Excess Non-Linearity. *IEEE Electron Device Letters*, **2020**, 41, 1750-1753	4.4	1
329	Improved TDDB Reliability and Interface States in 5-nm Hf0.5Zr0.5O2 Ferroelectric Technologies Using NH3 Plasma and Microwave Annealing. *IEEE Transactions on Electron Devices*, **2020**, 67, 1581-1585	2.9	16

328	A New 8T Hybrid Nonvolatile SRAM With Ferroelectric FET. *IEEE Journal of the Electron Devices Society*, **2020**, 8, 171-175	2.3	7
327	Compact Model for Geometry Dependent Mobility in Nanosheet FETs. *IEEE Electron Device Letters*, **2020**, 41, 313-316	4.4	6
326	Optimization of Negative-Capacitance Vertical-Tunnel FET (NCVT-FET). *IEEE Transactions on Electron Devices*, **2020**, 67, 2593-2599	2.9	26
325	Near Threshold Capacitance Matching in a Negative Capacitance FET With 1 nm Effective Oxide Thickness Gate Stack. *IEEE Electron Device Letters*, **2020**, 41, 179-182	4.4	16
324	BSIM Compact Model of Quantum Confinement in Advanced Nanosheet FETs. *IEEE Transactions on Electron Devices*, **2020**, 67, 730-737	2.9	16
323	Experimental Demonstration of a Ferroelectric HfO2-Based Content Addressable Memory Cell. *IEEE Electron Device Letters*, **2020**, 41, 240-243	4.4	28
322	Highly Scaled, High Endurance, Gate, Nanowire Ferroelectric FET Memory Transistors. *IEEE Electron Device Letters*, **2020**, 41, 1637-1640	4.4	22
321	**2020**,		3
320	Modeling of Current Mismatch and 1/f Noise for Halo-Implanted Drain-Extended MOSFETs. *IEEE Transactions on Electron Devices*, **2020**, 67, 4794-4801	2.9	0
319	Design Optimization Techniques in Nanosheet Transistor for RF Applications. *IEEE Transactions on Electron Devices*, **2020**, 67, 4515-4520	2.9	11
318	Analysis and Modeling of Polarization Gradient Effect on Negative Capacitance FET. *IEEE Transactions on Electron Devices*, **2020**, 67, 4521-4525	2.9	3
317	Enhanced ferroelectricity in ultrathin films grown directly on silicon. *Nature*, **2020**, 580, 478-482	50.4	232
316	. *IEEE Electron Device Letters*, **2019**, 40, 1423-1426	4.4	14
315	Ferroelectric Si-doped HfO2 Capacitors for Next-Generation Memories **2019**,		1
314	Effects of Annealing on Ferroelectric Hafnium Zirconium Oxide-Based Transistor Technology. *IEEE Electron Device Letters*, **2019**, 40, 467-470	4.4	17
313	Improved Modeling of Bulk Charge Effect for BSIM-BULK Model. *IEEE Transactions on Electron Devices*, **2019**, 66, 2850-2853	2.9	5
312	Characterization and Modeling of Flicker Noise in FinFETs at Advanced Technology Node. *IEEE Electron Device Letters*, **2019**, 40, 985-988	4.4	11
311	Spacer Engineering in Negative Capacitance FinFETs. *IEEE Electron Device Letters*, **2019**, 40, 1009-1012	4.4	18

310	Negative Capacitance FET With 1.8-nm-Thick Zr-Doped HfO2 Oxide. *IEEE Electron Device Letters*, **2019**, 40, 993-996	4.4	60
309	Optimization of NCFET by Matching Dielectric and Ferroelectric Nonuniformly Along the Channel. *IEEE Electron Device Letters*, **2019**, 40, 822-825	4.4	13
308	Evaluation of NC-FinFET Based Subsystem-Level Logic Circuits. *IEEE Transactions on Electron Devices*, **2019**, 66, 2004-2009	2.9	15
307	Analysis and Modeling of Inner Fringing Field Effect on Negative Capacitance FinFETs. *IEEE Transactions on Electron Devices*, **2019**, 66, 2023-2027	2.9	20
306	Accurate and Computationally Efficient Modeling of Nonquasi Static Effects in MOSFETs for Millimeter-Wave Applications. *IEEE Transactions on Electron Devices*, **2019**, 66, 44-51	2.9	6
305	Anomalously Beneficial Gate-Length Scaling Trend of Negative Capacitance Transistors. *IEEE Electron Device Letters*, **2019**, 40, 1860-1863	4.4	11
304	Monolithic 3D BEOL FinFET switch arrays using location-controlled-grain technique in voltage regulator with better FOM than 2D regulators **2019**,		8
303	Proposal for Capacitance Matching in Negative Capacitance Field-Effect Transistors. *IEEE Electron Device Letters*, **2019**, 40, 463-466	4.4	36
302	Spatially resolved steady-state negative capacitance. *Nature*, **2019**, 565, 468-471	50.4	144
301	Compact Modeling of Cross-Sectional Scaling in Gate-All-Around FETs: 3-D to 1-D Transition. *IEEE Transactions on Electron Devices*, **2018**, 65, 1094-1100	2.9	9
300	Designing 0.5 V 5-nm HP and 0.23 V 5-nm LP NC-FinFETs With Improved ${I}_{ mathrm{scriptscriptstyle OFF}}$ Sensitivity in Presence of Parasitic Capacitance. *IEEE Transactions on Electron Devices*, **2018**, 65, 1211-1216	2.9	22
299	Engineering Negative Differential Resistance in NCFETs for Analog Applications. *IEEE Transactions on Electron Devices*, **2018**, 65, 2033-2039	2.9	49
298	Improved Subthreshold Swing and Short Channel Effect in FDSOI n-Channel Negative Capacitance Field Effect Transistors. *IEEE Electron Device Letters*, **2018**, 39, 300-303	4.4	93
297	A Nitrided Interfacial Oxide for Interface State Improvement in Hafnium Zirconium Oxide-Based Ferroelectric Transistor Technology. *IEEE Electron Device Letters*, **2018**, 39, 95-98	4.4	20
296	NCFET Design Considering Maximum Interface Electric Field. *IEEE Electron Device Letters*, **2018**, 39, 1254-1257	4.4	19
295	Analysis and Modeling of Temperature and Bias Dependence of Current Mismatch in Halo-Implanted MOSFETs. *IEEE Transactions on Electron Devices*, **2018**, 65, 3608-3616	2.9	7
294	**2018**,		9
293	Negative-Capacitance FinFET Inverter, Ring Oscillator, SRAM Cell, and Ft **2018**,		14

292	Response Speed of Negative Capacitance FinFETs **2018**,		19
291	**2018**,		34
290	A Unified Flicker Noise Model for FDSOI MOSFETs Including Back-bias Effect **2018**,		4
289	Variation Caused by Spatial Distribution of Dielectric and Ferroelectric Grains in a Negative Capacitance Field-Effect Transistor. *IEEE Transactions on Electron Devices*, **2018**, 65, 4652-4658	2.9	15
288	UTBSOI MOSFET with corner spacers for energy-efficient applications **2018**,		3
287	Modeling of Induced Gate Thermal Noise Including Back-Bias Effect in FDSOI MOSFET. *IEEE Microwave and Wireless Components Letters*, **2018**, 28, 597-599	2.6	2
286	Anomalous Transconductance in Long Channel Halo Implanted MOSFETs: Analysis and Modeling. *IEEE Transactions on Electron Devices*, **2017**, 64, 376-383	2.9	11
285	A Predictive Tunnel FET Compact Model With Atomistic Simulation Validation. *IEEE Transactions on Electron Devices*, **2017**, 64, 599-605	2.9	18
284	Bulk FinFET With Low- $kappa $ Spacers for Continued Scaling. *IEEE Transactions on Electron Devices*, **2017**, 64, 1861-1864	2.9	23
283	Investigation of Mo/Ti/AlN/HfO2 High-k Metal Gate Stack for Low Power Consumption InGaAs NMOS Device Application. *IEEE Electron Device Letters*, **2017**, 38, 552-555	4.4	4
282	Compact Modeling of Drain Current Thermal Noise in FDSOI MOSFETs Including Back-Bias Effect. *IEEE Transactions on Microwave Theory and Techniques*, **2017**, 65, 2261-2270	4.1	8
281	Impact of Al content on InAs/AlSb/Alx Ga1⊠ Sb tunnelling diode. *Journal of Engineering*, **2017**, 2017, 403-406	0.7	
280	Self-Aligned, Gate Last, FDSOI, Ferroelectric Gate Memory Device With 5.5-nm Hf0.8Zr0.2O2, High Endurance and Breakdown Recovery. *IEEE Electron Device Letters*, **2017**, 38, 1379-1382	4.4	61
279	Compact Modeling Source-to-Drain Tunneling in Sub-10-nm GAA FinFET With Industry Standard Model. *IEEE Transactions on Electron Devices*, **2017**, 64, 3576-3581	2.9	10
278	High Vth enhancement mode GaN power devices with high ID, max using hybrid ferroelectric charge trap gate stack **2017**,		2
277	Modeling of Back-Gate Effects on Gate-Induced Drain Leakage and Gate Currents in UTB SOI MOSFETs. *IEEE Transactions on Electron Devices*, **2017**, 64, 3986-3990	2.9	7
276	Stabilization of ferroelectric phase in tungsten capped Hf0.8Zr0.2O2. *Applied Physics Letters*, **2017**, 111, 022907	3.4	36
275	High-gain monolithic 3D CMOS inverter using layered semiconductors. *Applied Physics Letters*, **2017**, 111, 222101	3.4	3

274	Nanowire FET With Corner Spacer for High-Performance, Energy-Efficient Applications. *IEEE Transactions on Electron Devices*, **2017**, 64, 5181-5187	2.9	16
273	Ferroelectricity in HfO2 thin films as a function of Zr doping **2017**,		2
272	FinFET With Encased Air-Gap Spacers for High-Performance and Low-Energy Circuits. *IEEE Electron Device Letters*, **2017**, 38, 16-19	4.4	27
271	Impact of Parasitic Capacitance and Ferroelectric Parameters on Negative Capacitance FinFET Characteristics. *IEEE Electron Device Letters*, **2017**, 38, 142-144	4.4	60
270	Differential voltage amplification from ferroelectric negative capacitance. *Applied Physics Letters*, **2017**, 111, 253501	3.4	27
269	Modeling of Charge and Quantum Capacitance in Low Effective Mass III-V FinFETs. *IEEE Journal of the Electron Devices Society*, **2016**, 4, 396-401	2.3	11
268	Study of Inherent Gate Coupling Nonuniformity of InAs/GaSb Vertical TFETs. *IEEE Transactions on Electron Devices*, **2016**, 63, 4267-4272	2.9	8
267	Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance—Part I: Model Description. *IEEE Transactions on Electron Devices*, **2016**, 63, 4981-4985	2.9	54
266	Methods for Extracting Flat Band Voltage in the InGaAs High Mobility Materials. *IEEE Electron Device Letters*, **2016**, 37, 1100-1103	4.4	7
265	Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance—Part II: Model Validation. *IEEE Transactions on Electron Devices*, **2016**, 63, 4986-4992	2.9	109
264	Modeling of threshold voltage for operating point using industry standard BSIM-IMG model **2016**,		5
263	FinFET With High- $kappa $ Spacers for Improved Drive Current. *IEEE Electron Device Letters*, **2016**, 37, 835-838	4.4	39
262	RF Modeling of FDSOI Transistors Using Industry Standard BSIM-IMG Model. *IEEE Transactions on Microwave Theory and Techniques*, **2016**, 64, 1745-1751	4.1	27
261	Monolithic 3D CMOS Using Layered Semiconductors. *Advanced Materials*, **2016**, 28, 2547-54	24	72
260	Effects of the Variation of Ferroelectric Properties on Negative Capacitance FET Characteristics. *IEEE Transactions on Electron Devices*, **2016**, 63, 2197-2199	2.9	103
259	Single crystal functional oxides on silicon. *Nature Communications*, **2016**, 7, 10547	17.4	106
258	Suppressing Non-Uniform Tunneling in InAs/GaSb TFET With Dual-Metal Gate. *IEEE Journal of the Electron Devices Society*, **2016**, 4, 60-65	2.3	17
257	Negative Capacitance in Short-Channel FinFETs Externally Connected to an Epitaxial Ferroelectric Capacitor. *IEEE Electron Device Letters*, **2016**, 37, 111-114	4.4	153

256	Compact models of negative-capacitance FinFETs: Lumped and distributed charge models **2016**,		55
255	Modeling of Subsurface Leakage Current in Low $V_{mathrm {TH}}$ Short Channel MOSFET at Accumulation Bias. *IEEE Transactions on Electron Devices*, **2016**, 63, 1840-1845	2.9	9
254	MoS2 transistors with 1-nanometer gate lengths. *Science*, **2016**, 354, 99-102	33.3	812
253	Corner spacer design for performance optimization of multi-gate InGaAs-OI FinFET with gate-to-source/drain underlap **2016**,		5
252	Quantum Well InAs/AlSb/GaSb Vertical Tunnel FET With HSQ Mechanical Support. *IEEE Nanotechnology Magazine*, **2015**, 14, 580-584	2.6	18
251	Modeling STI Edge Parasitic Current for Accurate Circuit Simulations. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 1291-1294	2.5	7
250	BSIM-IMG: Compact model for RF-SOI MOSFETs **2015**,		10
249	Piezoelectricity-Induced Schottky Barrier Height Variations in AlGaN/GaN High Electron Mobility Transistors. *IEEE Electron Device Letters*, **2015**, 36, 902-904	4.4	19
248	New industry standard FinFET compact model for future technology nodes **2015**,		10
247	Capacitance Modeling in III-V FinFETs. *IEEE Transactions on Electron Devices*, **2015**, 62, 3892-3897	2.9	18
246	2D layered materials: From materials properties to device applications **2015**,		8
245	Analytical Modeling of Flicker Noise in Halo Implanted MOSFETs. *IEEE Journal of the Electron Devices Society*, **2015**, 3, 355-360	2.3	16
244	Modeling SiGe FinFETs With Thin Fin and Current-Dependent Source/Drain Resistance. *IEEE Electron Device Letters*, **2015**, 36, 636-638	4.4	7
243	Electrostatic integrity and performance enhancement for UTB InGaAs-OI MOSFET with high-k dielectric through spacer design **2015**,		2
242	Sub-60mV-swing negative-capacitance FinFET without hysteresis **2015**,		123
241	Analytical Modeling and Experimental Validation of Threshold Voltage in BSIM6 MOSFET Model. *IEEE Journal of the Electron Devices Society*, **2015**, 3, 240-243	2.3	15
240	BSIM-CMG: Standard FinFET compact model for advanced circuit design **2015**,		27
239	Modeling 20-nm Germanium FinFET With the Industry Standard FinFET Model. *IEEE Electron Device Letters*, **2014**, 35, 711-713	4.4	18

238	Series resistance and mobility in mechanically-exfoliated layered transition metal dichalcogenide MOSFETs **2014**,		2
237	Modeling of GaN-Based Normally-Off FinFET. *IEEE Electron Device Letters*, **2014**, 35, 612-614	4.4	32
236	BSIM-IMG with improved surface potential calculation recipe **2014**,		5
235	Hybrid Si/TMD 2D electronic double channels fabricated using solid CVD few-layer-MoS2 stacking for Vth matching and CMOS-compatible 3DFETs **2014**,		10
234	Two-dimensional to three-dimensional tunneling in InAs/AlSb/GaSb quantum well heterojunctions. *Journal of Applied Physics*, **2013**, 114, 024502	2.5	12
233	Unified FinFET compact model: Modelling Trapezoidal Triple-Gate FinFETs **2013**,		20
232	Monolithic 3D chip integrated with 500ns NVM, 3ps logic circuits and SRAM **2013**,		24
231	Compact modeling for the changing transistor **2013**,		1
230	Low power negative capacitance FETs for future quantum-well body technology **2013**,		10
229	Device design considerations for ultra-thin body non-hysteretic negative capacitance FETs **2013**,		17
228	Interfacial layer reduction and high permittivity tetragonal ZrO2 on germanium reaching ultrathin 0.39 nm equivalent oxide thickness. *Applied Physics Letters*, **2013**, 102, 232906	3.4	15
227	Record-high 121/62 □A/□m on-currents 3D stacked epi-like Si FETs with and without metal back gate **2013**,		17
226	Random Telegraph Noise in 1X-nm CMOS Silicide Contacts and a Method to Extract Trap Density. *IEEE Electron Device Letters*, **2012**, 33, 591-593	4.4	1
225	Denser and More Stable SRAM Using FinFETs With Multiple Fin Heights. *IEEE Transactions on Electron Devices*, **2012**, 59, 2037-2041	2.9	36
224	A little known benefit of FinFET over Planar MOSFET in highperformance circuits at advanced technology nodes **2012**,		6
223	A non-iterative physical procedure for RF CMOS compact model extraction using BSIM6 **2012**,		9
222	Fast programming metal-gate Si quantum dot nonvolatile memory using green nanosecond laser spike annealing. *Applied Physics Letters*, **2012**, 100, 143501	3.4	32
221	Threshold Vacuum Switch (TVS) on 3D-stackable and 4F2 cross-point bipolar and unipolar resistive random access memory **2012**,		4

220	3D Ferroelectric-like NVM/CMOS hybrid chip by sub-400 ℃ sequential layered integration **2012**,		3
219	Denser and more stable FinFET SRAM using multiple fin heights **2011**,		1
218	A Novel Nanoinjection Lithography (NInL) Technology and Its Application for 16-nm Node Device Fabrication. *IEEE Transactions on Electron Devices*, **2011**, 58, 3678-3686	2.9	5
217	Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation **2011**,		180
216	BSIM-CG: A compact model of cylindrical gate / nanowire MOSFETs for circuit simulations **2011**,		1
215	Modeling intrinsic and extrinsic asymmetry of 3D cylindrical gate/gate-all-around FETs for circuit simulations **2011**,		3
214	Bifacial CIGS (11% efficiency)/Si solar cells by Cd-free and sodium-free green process integrated with CIGS TFTs **2011**,		3
213	Ultrathin body InAs tunneling field-effect transistors on Si substrates. *Applied Physics Letters*, **2011**, 98, 113105	3.4	69
212	Novel 140℃ hybrid thin film solar cell/transistor technology with 9.6% conversion efficiency and 1.1 cm2/V-s electron mobility for low-temperature substrates **2010**,		1
211	Tunnel Field Effect Transistor With Raised Germanium Source. *IEEE Electron Device Letters*, **2010**, 31, 1107-1109	4.4	113
210	Global parameter extraction for a multi-gate MOSFETs compact model **2010**,		11
209	Prospect of tunneling green transistor for 0.1V CMOS **2010**,		47
208	Cycling induced degradation of a 65nm FPGA flash memory switch **2010**,		2
207	16nm functional 0.039μm2 6T-SRAM cell with nano injection lithography, nanowire channel, and full TiN gate **2009**,		2
206	Air-Spacer MOSFET With Self-Aligned Contact for Future Dense Memories. *IEEE Electron Device Letters*, **2009**, 30, 1368-1370	4.4	17
205	Design of FinFET SRAM Cells Using a Statistical Compact Model **2009**,		13
204	A Low Voltage Steep Turn-Off Tunnel Transistor Design **2009**,		15
203	Gate last MOSFET with air spacer and self-aligned contacts for dense memories **2009**,		2

202	Flicker-Noise Impact on Scaling of Mixed-Signal CMOS With HfSiON. *IEEE Transactions on Electron Devices*, **2008**, 55, 417-422	2.9	9
201	Feedback FET: A novel transistor exhibiting steep switching behavior at low bias voltages **2008**,		55
200	Green transistor as a solution to the IC power crisis **2008**,		29
199	Green Transistor - A VDD Scaling Path for Future Low Power ICs. *International Power Modulator Symposium and High-Voltage Workshop*, **2008**,		15
198	Air spacer MOSFET technology for 20nm node and beyond **2008**,		4
197	Statistical Compact Modeling of Variations in Nano MOSFETs **2008**,		6
196	Low-voltage green transistor using hetero-tunneling **2008**,		2
195	Low-voltage green transistor using ultra shallow junction and hetero-tunneling **2008**,		17
194	Effect of Top Electrode Material on Resistive Switching Properties of $hbox{ZrO}_{2}$ Film Memory Devices. *IEEE Electron Device Letters*, **2007**, 28, 366-368	4.4	262
193	Modified resistive switching behavior of ZrO2 memory films based on the interface layer formed by using Ti top electrode. *Journal of Applied Physics*, **2007**, 102, 094101	2.5	119
192	Random telegraph noise in flash memories - model and technology scaling **2007**,		84
191	A Multi-Gate MOSFET Compact Model Featuring Independent-Gate Operation **2007**,		17
190	BSIM-MG: A Versatile Multi-Gate FET Model for Mixed-Signal Design **2007**,		31
189	MOSFET design for forward body biasing scheme. *IEEE Electron Device Letters*, **2006**, 27, 387-389	4.4	26
188	MOSFET hot-carrier reliability improvement by forward-body bias. *IEEE Electron Device Letters*, **2006**, 27, 605-608	4.4	12
187	Effect of Fluorine Incorporation on 1/f Noise of HfSiON FETs for Future Mixed-Signal CMOS **2006**,		6
186	Bias polarity dependent effects of P+floating gate EEPROMs. *IEEE Transactions on Electron Devices*, **2004**, 51, 282-285	2.9	8
185	Characterization of spatial intrafield gate CD variability, its impact on circuit performance, and spatial mask-level correction. *IEEE Transactions on Semiconductor Manufacturing*, **2004**, 17, 2-11	2.6	54

184	MOSFET gate leakage modeling and selection guide for alternative gate dielectrics based on leakage considerations. *IEEE Transactions on Electron Devices*, **2003**, 50, 1027-1035	2.9	141
183	Loop-based interconnect modeling and optimization approach for multigigahertz clock network design. *IEEE Journal of Solid-State Circuits*, **2003**, 38, 457-463	5.5	15
182	Improved a priori interconnect predictions and technology extrapolation in the GTX system. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2003**, 11, 3-14	2.6	6
181	Frequency-independent equivalent-circuit model for on-chip spiral inductors. *IEEE Journal of Solid-State Circuits*, **2003**, 38, 419-426	5.5	212
180	RF characterization of metal T-gate structure in fully-depleted SOI CMOS technology. *IEEE Electron Device Letters*, **2003**, 24, 251-253	4.4	5
179	On the body-source built-in potential lowering of SOI MOSFETs. *IEEE Electron Device Letters*, **2003**, 24, 90-92	4.4	8
178	Direct tunneling RAM (DT-RAM) for high-density memory applications. *IEEE Electron Device Letters*, **2003**, 24, 475-477	4.4	2
177	Design and fabrication of 50-nm thin-body p-MOSFETs with a SiGe heterostructure channel. *IEEE Transactions on Electron Devices*, **2002**, 49, 279-286	2.9	25
176	A spacer patterning technology for nanoscale CMOS. *IEEE Transactions on Electron Devices*, **2002**, 49, 436-441	2.9	144
175	A simple method for optimization of 6H-SiC punch-through junctions used in both unipolar and bipolar power devices. *IEEE Transactions on Electron Devices*, **2002**, 49, 933-937	2.9	3
174	Equivalent junction method to predict 3-D effect of curved-abrupt p-n junctions. *IEEE Transactions on Electron Devices*, **2002**, 49, 1322-1325	2.9	37
173	Direct-tunneling gate leakage current in double-gate and ultrathin body MOSFETs. *IEEE Transactions on Electron Devices*, **2002**, 49, 2288-2295	2.9	55
172	Dual work function metal gate CMOS transistors by Ni-Ti interdiffusion. *IEEE Electron Device Letters* , **2002**, 23, 200-202	4.4	59
171	Direct tunneling leakage current and scalability of alternative gate dielectrics. *Applied Physics Letters*, **2002**, 81, 2091-2093	3.4	162
170	JVD silicon nitride as tunnel dielectric in p-channel flash memory. *IEEE Electron Device Letters*, **2002**, 23, 91-93	4.4	14
169	Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology. *Journal of Applied Physics*, **2002**, 92, 7266-7271	2.5	362
168	A thermal activation view of low voltage impact ionization in MOSFETs. *IEEE Electron Device Letters*, **2002**, 23, 550-552	4.4	20
167	Effects of high-/spl kappa/ gate dielectric materials on metal and silicon gate workfunctions. *IEEE Electron Device Letters*, **2002**, 23, 342-344	4.4	140

166	Impact of spatial intrachip gate length variability on the performance of high-speed digital circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2002**, 21, 544-553	2.5	88
165	Nanoscale CMOS spacer FinFET for the terabit era. *IEEE Electron Device Letters*, **2002**, 23, 25-27	4.4	124
164	Effective on-chip inductance modeling for multiple signal lines and application to repeater insertion. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2002**, 10, 799-805	2.6	20
163	An adjustable work function technology using Mo gate for CMOS devices. *IEEE Electron Device Letters*, **2002**, 23, 49-51	4.4	139
162	Normalized mutual integral difference method to extract threshold voltage of MOSFETs. *IEEE Electron Device Letters*, **2002**, 23, 428-430	4.4	15
161	Scaling CMOS devices through alternative structures. *Science in China Series F: Information Sciences*, **2001**, 44, 1-7		1
160	Charge-trap memory device fabricated by oxidation of Si/sub 1-x/Ge/sub x/. *IEEE Transactions on Electron Devices*, **2001**, 48, 696-700	2.9	204
159	SOI thermal impedance extraction methodology and its significance for circuit simulation. *IEEE Transactions on Electron Devices*, **2001**, 48, 730-736	2.9	111
158	Noise modeling and characterization for 1.5-V 1.8-GHz SOI low-noise amplifier. *IEEE Transactions on Electron Devices*, **2001**, 48, 803-809	2.9	6
157	Patterning sub-30-nm MOSFET gate with i-line lithography. *IEEE Transactions on Electron Devices*, **2001**, 48, 1004-1006	2.9	29
156	Optimization of sub-5-nm multiple-thickness gate oxide formed by oxygen implantation. *IEEE Transactions on Electron Devices*, **2001**, 48, 1279-1281	2.9	4
155	Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron and hole tunneling. *IEEE Transactions on Electron Devices*, **2001**, 48, 1366-1373	2.9	226
154	Dual work function metal gate CMOS technology using metal interdiffusion. *IEEE Electron Device Letters*, **2001**, 22, 444-446	4.4	140
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46	MOS memory using germanium nanocrystals formed by thermal oxidation of Si/sub 1-x/Ge/sub x/		3
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42	Threshold voltage shift by quantum confinement in ultra-thin body device		2
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37	RLC signal integrity analysis of high-speed global interconnects [CMOS]	6
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30	FinFET-a quasi-planar double-gate MOSFET	12
29	Metal gate work function adjustment for future CMOS technology	1
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26	Design analysis of thin-body silicide source/drain devices	9
25	Quasi-planar NMOS FinFETs with sub-100 nm gate lengths	9
24	Modeling and design study of nanocrystal memory devices	1
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22	An effective gate resistance model for CMOS RF and noise modeling	1
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