Chenming Hu

List of Publications by Citations

345 papers	14,645 citations	57 h-index	112 g-index
397 ext. papers	17,385 ext. citations	4.2 avg, IF	6.32 L-index

#	Paper	IF	Citations
345	FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. *IEEE Transactions on Electron Devices*, **2000**, 47, 2320-2325	2.9	1005
344	MoS2 transistors with 1-nanometer gate lengths. *Science*, **2016**, 354, 99-102	33.3	812
343	Hot-electron-induced MOSFET degradation Model, monitor, and improvement. *IEEE Transactions on Electron Devices*, **1985**, 32, 375-385	2.9	639
342	. *IEEE Transactions on Electron Devices*, **1994**, 41, 761-767	2.9	413
341	MOS capacitance measurements for high-leakage thin dielectrics. *IEEE Transactions on Electron Devices*, **1999**, 46, 1500-1501	2.9	401
340	Electrical breakdown in thin gate and tunneling oxides. *IEEE Transactions on Electron Devices*, **1985**, 32, 413-422	2.9	388
339	Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology. *Journal of Applied Physics*, **2002**, 92, 7266-7271	2.5	362
338	Effect of Top Electrode Material on Resistive Switching Properties of $hbox{ZrO}_{2}$ Film Memory Devices. *IEEE Electron Device Letters*, **2007**, 28, 366-368	4.4	262
337	Hot-electron-induced photon and photocarrier generation in Silicon MOSFET's. *IEEE Transactions on Electron Devices*, **1984**, 31, 1264-1273	2.9	240
336	Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI. *IEEE Transactions on Electron Devices*, **1997**, 44, 414-422	2.9	233
335	Enhanced ferroelectricity in ultrathin films grown directly on silicon. *Nature*, **2020**, 580, 478-482	50.4	232
334	Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron and hole tunneling. *IEEE Transactions on Electron Devices*, **2001**, 48, 1366-1373	2.9	226
333	Frequency-independent equivalent-circuit model for on-chip spiral inductors. *IEEE Journal of Solid-State Circuits*, **2003**, 38, 419-426	5.5	212
332	Charge-trap memory device fabricated by oxidation of Si/sub 1-x/Ge/sub x/. *IEEE Transactions on Electron Devices*, **2001**, 48, 696-700	2.9	204
331	Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation **2011**,		180
330	Hot-Electron-Induced MOSFET Degradation - Model, Monitor, and Improvement. *IEEE Journal of Solid-State Circuits*, **1985**, 20, 295-305	5.5	169
329	Direct tunneling leakage current and scalability of alternative gate dielectrics. *Applied Physics Letters*, **2002**, 81, 2091-2093	3.4	162

328	Negative Capacitance in Short-Channel FinFETs Externally Connected to an Epitaxial Ferroelectric Capacitor. *IEEE Electron Device Letters*, **2016**, 37, 111-114	4.4	153
327	Quantum yield of electron impact ionization in silicon. *Journal of Applied Physics*, **1985**, 57, 302-309	2.5	151
326	A spacer patterning technology for nanoscale CMOS. *IEEE Transactions on Electron Devices*, **2002**, 49, 436-441	2.9	144
325	Spatially resolved steady-state negative capacitance. *Nature*, **2019**, 565, 468-471	50.4	144
324	MOSFET gate leakage modeling and selection guide for alternative gate dielectrics based on leakage considerations. *IEEE Transactions on Electron Devices*, **2003**, 50, 1027-1035	2.9	141
323	Dual work function metal gate CMOS technology using metal interdiffusion. *IEEE Electron Device Letters*, **2001**, 22, 444-446	4.4	140
322	Effects of high-/spl kappa/ gate dielectric materials on metal and silicon gate workfunctions. *IEEE Electron Device Letters*, **2002**, 23, 342-344	4.4	140
321	An adjustable work function technology using Mo gate for CMOS devices. *IEEE Electron Device Letters*, **2002**, 23, 49-51	4.4	139
320	Ultrathin-body SOI MOSFET for deep-sub-tenth micron era. *IEEE Electron Device Letters*, **2000**, 21, 254-255	4.4	134
319	Lucky-electron model of channel hot-electron injection in MOSFET'S. *IEEE Transactions on Electron Devices*, **1984**, 31, 1116-1125	2.9	132
318	Nanoscale CMOS spacer FinFET for the terabit era. *IEEE Electron Device Letters*, **2002**, 23, 25-27	4.4	124
317	Sub-60mV-swing negative-capacitance FinFET without hysteresis **2015**,		123
316	Modified resistive switching behavior of ZrO2 memory films based on the interface layer formed by using Ti top electrode. *Journal of Applied Physics*, **2007**, 102, 094101	2.5	119
315	Short-channel effect improved by lateral channel-engineering in deep-submicronmeter MOSFET's. *IEEE Transactions on Electron Devices*, **1997**, 44, 627-634	2.9	114
314	Tunnel Field Effect Transistor With Raised Germanium Source. *IEEE Electron Device Letters*, **2010**, 31, 1107-1109	4.4	113
313	A physical and scalable I-V model in BSIM3v3 for analog/digital circuit simulation. *IEEE Transactions on Electron Devices*, **1997**, 44, 277-287	2.9	112
312	Inversion-layer capacitance and mobility of very thin gate-Oxide MOSFET's. *IEEE Transactions on Electron Devices*, **1986**, 33, 409-413	2.9	112
311	SOI thermal impedance extraction methodology and its significance for circuit simulation. *IEEE Transactions on Electron Devices*, **2001**, 48, 730-736	2.9	111

310	Direct tunneling gate leakage current in transistors with ultrathin silicon nitride gate dielectric. *IEEE Electron Device Letters*, **2000**, 21, 540-542	4.4	110
309	Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance—Part II: Model Validation. *IEEE Transactions on Electron Devices*, **2016**, 63, 4986-4992	2.9	109
308	Metal-oxide-semiconductor field-effect-transistor substrate current during Fowler–Nordheim tunneling stress and silicon dioxide reliability. *Journal of Applied Physics*, **1994**, 76, 3695-3700	2.5	107
307	Single crystal functional oxides on silicon. *Nature Communications*, **2016**, 7, 10547	17.4	106
306	Effects of the Variation of Ferroelectric Properties on Negative Capacitance FET Characteristics. *IEEE Transactions on Electron Devices*, **2016**, 63, 2197-2199	2.9	103
305	Sub-60-nm quasi-planar FinFETs fabricated using a simplified process. *IEEE Electron Device Letters*, **2001**, 22, 487-489	4.4	99
304	Transistor characteristics with Ta/sub 2/O/sub 5/ gate dielectric. *IEEE Electron Device Letters*, **1998**, 19, 441-443	4.4	96
303	Complementary silicide source/drain thin-body MOSFETs for the 20 nm gate length regime		96
302	Improved Subthreshold Swing and Short Channel Effect in FDSOI n-Channel Negative Capacitance Field Effect Transistors. *IEEE Electron Device Letters*, **2018**, 39, 300-303	4.4	93
301	MOSFET degradation due to stressing of thin oxide. *IEEE Transactions on Electron Devices*, **1984**, 31, 1238-1244	2.9	93
300	Impact of spatial intrachip gate length variability on the performance of high-speed digital circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2002**, 21, 544-553	2.5	88
299	Random telegraph noise in flash memories - model and technology scaling **2007**,		84
298	Dual-metal gate CMOS technology with ultrathin silicon nitride gate dielectric. *IEEE Electron Device Letters*, **2001**, 22, 227-229	4.4	83
297	Optimum doping profile for minimum ohmic resistance and high-breakdown voltage. *IEEE Transactions on Electron Devices*, **1979**, 26, 243-244	2.9	77
296	Monolithic 3D CMOS Using Layered Semiconductors. *Advanced Materials*, **2016**, 28, 2547-54	24	72
295	Ultrathin body InAs tunneling field-effect transistors on Si substrates. *Applied Physics Letters*, **2011**, 98, 113105	3.4	69
294	Characterization of self-heating in advanced VLSI interconnect lines based on thermal finite element simulation. *IEEE Transactions on Components and Packaging Technologies*, **1998**, 21, 406-411		69
293	Self-Aligned, Gate Last, FDSOI, Ferroelectric Gate Memory Device With 5.5-nm Hf0.8Zr0.2O2, High Endurance and Breakdown Recovery. *IEEE Electron Device Letters*, **2017**, 38, 1379-1382	4.4	61

292	Negative Capacitance FET With 1.8-nm-Thick Zr-Doped HfO2 Oxide. *IEEE Electron Device Letters*, **2019**, 40, 993-996	4.4	60
291	Impact of Parasitic Capacitance and Ferroelectric Parameters on Negative Capacitance FinFET Characteristics. *IEEE Electron Device Letters*, **2017**, 38, 142-144	4.4	60
290	Dual work function metal gate CMOS transistors by Ni-Ti interdiffusion. *IEEE Electron Device Letters* , **2002**, 23, 200-202	4.4	59
289	A robust and physical BSIM3 non-quasi-static transient and AC small-signal model for circuit simulation. *IEEE Transactions on Electron Devices*, **1998**, 45, 834-841	2.9	58
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287	Electrical Breakdown in Thin Gate and Tunneling Oxides. *IEEE Journal of Solid-State Circuits*, **1985**, 20, 333-342	5.5	57
286	A 0.1-/spl mu/m delta-doped MOSFET fabricated with post-low-energy implanting selective epitaxy. *IEEE Transactions on Electron Devices*, **1998**, 45, 809-814	2.9	56
285	Leakage current comparison between ultra-thin Ta2O5 films and conventional gate dielectrics. *IEEE Electron Device Letters*, **1998**, 19, 341-342	4.4	56
284	Gate engineering for deep-submicron CMOS transistors. *IEEE Transactions on Electron Devices*, **1998** , 45, 1253-1262	2.9	55
283	Feedback FET: A novel transistor exhibiting steep switching behavior at low bias voltages **2008**,		55
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281	Hot-carrier-induced MOSFET degradation under AC stress. *IEEE Electron Device Letters*, **1987**, 8, 333-335	4.4	55
280	Compact models of negative-capacitance FinFETs: Lumped and distributed charge models **2016**,		55
279	Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance—Part I: Model Description. *IEEE Transactions on Electron Devices*, **2016**, 63, 4981-4985	2.9	54
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271	High-current failure model for VLSI interconnects under short-pulse stress conditions. *IEEE Electron Device Letters*, **1997**, 18, 405-407	4.4	48
270	Prospect of tunneling green transistor for 0.1V CMOS **2010**,		47
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268	Liquid-crystal waveguides for integrated optics. *IEEE Journal of Quantum Electronics*, **1977**, 13, 262-267	2	47
267	Correlation between substrate and gate currents in MOSFET's. *IEEE Transactions on Electron Devices*, **1982**, 29, 1740-1744	2.9	45
266	An analytical breakdown model for short-channel MOSFET's. *IEEE Transactions on Electron Devices*, **1982**, 29, 1735-1740	2.9	44
265	On thermal effects in deep sub-micron VLSI interconnects		41
264	FinFET With High- $kappa $ Spacers for Improved Drive Current. *IEEE Electron Device Letters*, **2016**, 37, 835-838	4.4	39
263	Nanoscale ultra-thin-body silicon-on-insulator P-MOSFET with a SiGe/Si heterostructure channel. *IEEE Electron Device Letters*, **2000**, 21, 161-163	4.4	39
262	Sub 50-nm FinFET: PMOS		39
261	Equivalent junction method to predict 3-D effect of curved-abrupt p-n junctions. *IEEE Transactions on Electron Devices*, **2002**, 49, 1322-1325	2.9	37
260	Denser and More Stable SRAM Using FinFETs With Multiple Fin Heights. *IEEE Transactions on Electron Devices*, **2012**, 59, 2037-2041	2.9	36
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257	Proposal for Capacitance Matching in Negative Capacitance Field-Effect Transistors. *IEEE Electron Device Letters*, **2019**, 40, 463-466	4.4	36

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253	Modeling of GaN-Based Normally-Off FinFET. *IEEE Electron Device Letters*, **2014**, 35, 612-614	4.4	32
252	Fast programming metal-gate Si quantum dot nonvolatile memory using green nanosecond laser spike annealing. *Applied Physics Letters*, **2012**, 100, 143501	3.4	32
251	Nanoscale ultrathin body PMOSFETs with raised selective germanium source/drain. *IEEE Electron Device Letters*, **2001**, 22, 447-448	4.4	32
250	Electron trapping in very thin thermal silicon dioxides **1981**,		32
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248	The effect of interconnect scaling and low-k dielectric on the thermal characteristics of the IC metal		31
247	A parametric study of power MOSFETs **1979**,		31
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244	Patterning sub-30-nm MOSFET gate with i-line lithography. *IEEE Transactions on Electron Devices*, **2001**, 48, 1004-1006	2.9	29
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235	Modeling and characterization of electromigration failures under bidirectional current stress. *IEEE Transactions on Electron Devices*, **1996**, 43, 800-808	2.9	27
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229	Bulk FinFET With Low- $kappa $ Spacers for Continued Scaling. *IEEE Transactions on Electron Devices*, **2017**, 64, 1861-1864	2.9	23
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223	Analysis and Modeling of Inner Fringing Field Effect on Negative Capacitance FinFETs. *IEEE Transactions on Electron Devices*, **2019**, 66, 2023-2027	2.9	20
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