Patrick Girard

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/7526804/publications.pdf

Version: 2024-02-01

36	467	759233 12	752698 20
papers	citations	h-index	g-index

37	37	37	153
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Novel Quadruple-Node-Upset-Tolerant Latch Designs With Optimized Overhead for Reliable Computing in Harsh Radiation Environments. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 404-413.	4.6	49
2	Cost-Effective and Highly Reliable Circuit-Components Design for Safety-Critical Applications. IEEE Transactions on Aerospace and Electronic Systems, 2022, 58, 517-529.	4.7	20
3	All-spin PUF: An Area-efficient and Reliable PUF Design with Signature Improvement for Spin-transfer Torque Magnetic Cell-based All-spin Circuits. ACM Journal on Emerging Technologies in Computing Systems, 2022, 18, 1-20.	2.3	2
4	Quadruple and Sextuple Cross-Coupled SRAM Cell Designs With Optimized Overhead for Reliable Applications. IEEE Transactions on Device and Materials Reliability, 2022, 22, 282-295.	2.0	34
5	SCLCRL: Shuttling C-elements based Low-Cost and Robust Latch Design Protected against Triple Node Upsets in Harsh Radiation Environments. , 2022, , .		3
6	Designs of Level-Sensitive T Flip-Flops and Polar Encoders Based on Two XOR/XNOR Gates. Electronics (Switzerland), 2022, 11, 1658.	3.1	5
7	Two 0.8 V, Highly Reliable RHBD 10T and 12T SRAM Cells for Aerospace Applications. , 2022, , .		0
8	Sextuple Cross-Coupled-DICE Based Double-Node-Upset Recoverable and Low-Delay Flip-Flop for Aerospace Applications. , 2022, , .		0
9	A Highly Robust, Low Delay and DNU-Recovery Latch Design for Nanoscale CMOS Technology. , 2022, , .		1
10	A Highly Reliable and Low Power RHBD Flip-Flop Cell for Aerospace Applications. , 2022, , .		1
11	A Survey of Test and Reliability Solutions for Magnetic Random Access Memories. Proceedings of the IEEE, 2021, 109, 149-169.	21.3	24
12	Improving TID Radiation Robustness of a CMOS OxRAM-Based Neuron Circuit by Using Enclosed Layout Transistors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1122-1131.	3.1	11
13	DOVA PRO: A Dynamic Overwriting Voltage Adjustment Technique for STT-MRAM L1 Cache Considering Dielectric Breakdown Effect. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1325-1334.	3.1	2
14	Error-Tolerant Reconfigurable VDD 10T SRAM Architecture for IoT Applications. Electronics (Switzerland), 2021, 10, 1718.	3.1	4
15	Multi-Level Control of Resistive RAM (RRAM) Using a Write Termination to Achieve 4 Bits/Cell in High Resistance State. Electronics (Switzerland), 2021, 10, 2222.	3.1	9
16	A Novel Low-Cost TMR-Without-Voter Based HIS-Insensitive and MNU-Tolerant Latch Design for Aerospace Applications. IEEE Transactions on Aerospace and Electronic Systems, 2020, 56, 2666-2676.	4.7	24
17	Quadruple Cross-Coupled Dual-Interlocked-Storage-Cells-Based Multiple-Node-Upset-Tolerant Latch Designs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 879-890.	5.4	32
18	A CMOS OxRAM-Based Neuron Circuit Hardened with Enclosed Layout Transistors for Aerospace Applications. , 2020, , .		2

#	Article	IF	Citations
19	DOVA: A Dynamic Overwriting Voltage Adjustment for STT-RAM L1 Cache. , 2020, , .		1
20	HITTSFL: Design of a Cost-Effective HIS-Insensitive TNU-Tolerant and SET-Filterable Latch for Safety-Critical Applications. , 2020, , .		3
21	Design of a Highly Reliable SRAM Cell with Advanced Self-Recoverability from Soft Errors. , 2020, , .		6
22	Novel Speed-and-Power-Optimized SRAM Cell Designs With Enhanced Self-Recoverability From Single- and Double-Node Upsets. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4684-4695.	5.4	50
23	Cell-Aware Defect Diagnosis of Customer Returns Based on Supervised Learning. IEEE Transactions on Device and Materials Reliability, 2020, 20, 329-340.	2.0	7
24	A Survey of Testing Techniques for Approximate Integrated Circuits. Proceedings of the IEEE, 2020, 108, 2178-2194.	21.3	15
25	Information Assurance Through Redundant Design: A Novel TNU Error-Resilient Latch for Harsh Radiation Environment. IEEE Transactions on Computers, 2020, 69, 789-799.	3.4	66
26	A Sextuple Cross-Coupled SRAM Cell Protected against Double-Node Upsets. , 2020, , .		3
27	A Test Pattern Generation Technique for Approximate Circuits Based on an ILP-Formulated Pattern Selection Procedure. IEEE Nanotechnology Magazine, 2019, 18, 849-857.	2.0	13
28	Novel Radiation Hardened Latch Design with Cost-Effectiveness for Safety-Critical Terrestrial Applications. , 2019, , .		1
29	Novel Quadruple Cross-Coupled Memory Cell Designs With Protection Against Single Event Upsets and Double-Node Upsets. IEEE Access, 2019, 7, 176188-176196.	4.2	20
30	Design of a Sextuple Cross-Coupled SRAM Cell with Optimized Access Operations for Highly Reliable Terrestrial Applications. , 2019, , .		4
31	Testing approximate digital circuits: Challenges and opportunities. , 2018, , .		16
32	Investigation of Mean-Error Metrics for Testing Approximate Integrated Circuits. , 2018, , .		8
33	Towards digital circuit approximation by exploiting fault simulation. , 2017, , .		5
34	Dynamic Compact Model of Self-Referenced Magnetic Tunnel Junction. IEEE Transactions on Electron Devices, 2014, 61, 3877-3882.	3.0	2
35	A Complete Resistive-Open Defect Analysis for Thermally Assisted Switching MRAMs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2326-2335.	3.1	20
36	Design of Radiation Hardened Latch and Flip-Flop with Cost-Effectiveness for Low-Orbit Aerospace Applications. Journal of Electronic Testing: Theory and Applications (JETTA), 0, , 1.	1.2	4