Jose C A P Monteiro

List of Publications by Year
in descending order

110 papers	1,437 citations	687363 13 h-index	526287 27 g-index
114 all docs	114 docs citations	114 times ranked	445 citing authors

#	Article	IF	Citations
1	A distributed Monte Carlo based linear algebra solver applied to the analysis of large complex networks. Future Generation Computer Systems, 2022, 127, 320-330.	7.5	4
2	A Review of Synthetic-Aperture Radar Image Formation Algorithms and Implementations: A Computational Perspective. Remote Sensing, 2022, 14, 1258.	4.0	20
3	A rare sporadic pancreatic desmoid fibromatosis with splenic vein invasion diagnosed by CT scan-guided core needle biopsy: a case report with possible differential diagnosis from metastatic colorectal or renal cancer. Journal of Surgical Case Reports, 2021, 2021, rjab257.	0.4	2
4	A systematic review and meta-analysis of the safety and efficacy of endoscopic enucleation and non-enucleation procedures for benign prostatic enlargement. World Journal of Urology, 2020, 38, 1663-1684.	2.2	16
5	A highly parallel algorithm for computing the action of a matrix exponential on a vector based on a multilevel Monte Carlo method. Computers and Mathematics With Applications, 2020, 79, 3495-3515.	2.7	6
6	Radixâ€2 ^r recoding with common subexpression elimination for multiple constant multiplication. IET Circuits, Devices and Systems, 2020, 14, 990-994.	1.4	1
7	Short-circuit Analysis using a Parallel QBF Solver. , 2020, , .		0
8	Analysis of short-circuit conditions in logic circuits. , 2017, , .		3
9	A novel method for the approximation of multiplierless constant matrix vector multiplication. Eurasip Journal on Embedded Systems, 2016, 2016, .	1.2	6
10	Power Analysis and Optimization from Circuitto Register-Transfer Levels. , 2016, , 57-76.		0
11	Automatic equivalence checking of programs with uninterpreted functions and integer arithmetic. International Journal on Software Tools for Technology Transfer, 2016, 18, 359-374.	1.9	18
12	A Novel Method for the Approximation of Multiplierless Constant Matrix Vector Multiplication. , 2015, , .		2
13	Approximation of multiple constant multiplications using minimum look-up tables on FPGA. , 2015, , .		3
14	Exact and Approximate Algorithms for the Filter Design Optimization Problem. IEEE Transactions on Signal Processing, 2015, 63, 142-154.	5.3	12
15	Quaternary Logic Lookup Table in Standard CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 306-316.	3.1	14
16	Multiplierless Design of Folded DSP Blocks. ACM Transactions on Design Automation of Electronic Systems, 2014, 20, 1-24.	2.6	6
17	Optimization of design complexity in time-multiplexed constant multiplications. , 2014, , .		0
18	ECHO: A novel method for the multiplierless design of constant array vector multiplication. , 2014, , .		3

#	Article	IF	Citations
19	Efficient design of FIR filters using hybrid multiple constant multiplications on FPGA. , 2014, , .		5
20	A Tutorial on Multiplierless Design of FIR Filters: Algorithms and Architectures. Circuits, Systems, and Signal Processing, 2014, 33, 1689-1719.	2.0	32
21	Optimization of design complexity in time-multiplexed constant multiplications. , 2014, , .		1
22	Weakest Precondition Synthesis for Compiler Optimizations. Lecture Notes in Computer Science, 2014, , 203-221.	1.3	10
23	Standard CMOS voltage-mode QLUT using a clock boosting technique. , 2013, , .		0
24	Towards the least complex time-multiplexed constant multiplication. , 2013, , .		0
25	Exploration of tradeoffs in the design of integer cosine transforms for image compression. , 2013, , .		0
26	Design of Digit-Serial FIR Filters: Algorithms, Architectures, and a CAD Tool. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 498-511.	3.1	23
27	SIREN. , 2013, , .		1
28	Coverage-directed observability-based validation for embedded software. ACM Transactions on Design Automation of Electronic Systems, 2013, 18, 1-20.	2.6	1
29	Optimization Algorithms for the Multiplierless Realization of Linear Transforms. ACM Transactions on Design Automation of Electronic Systems, 2012, 17, 1-27.	2.6	15
30	Multiple tunable constant multiplications. , 2012, , .		6
31	Efficient area and power multiplication part of FFT based on twiddle factor decomposition. , 2012, , .		3
32	Hardware pipelining of runtime-detected loops. , 2012, , .		1
33	Design and characterization of a QLUT in a standard CMOS process. , 2012, , .		1
34	Design of low-complexity digital finite impulse response filters on FPGAs. , 2012, , .		6
35	High-level algorithms for the optimization of gate-level area in digit-serial multiple constant multiplications. The Integration VLSI Journal, 2012, 45, 294-306.	2.1	4
36	Analysis of the conditions for the worst case switching activity in integrated circuits. Analog Integrated Circuits and Signal Processing, 2012, 70, 229-240.	1.4	0

#	Article	IF	Citations
37	Multiplierless Design of Linear DSP Transforms. International Federation for Information Processing, 2012, , 73-93.	0.4	11
38	A hybrid algorithm for the optimization of area and delay in linear DSP transforms. , 2011, , .		1
39	Optimization of area in digit-serial Multiple Constant Multiplications at gate-level. , 2011, , .		10
40	Design of low-power multiple constant multiplications using low-complexity minimum depth operations. , 2011, , .		7
41	Finding the optimal tradeoff between area and delay in multiple constant multiplications. Microprocessors and Microsystems, 2011, 35, 729-741.	2.8	16
42	Efficient shift-adds design of digit-serial multiple constant multiplications. , 2011, , .		8
43	Optimization of gate-level area in high throughput Multiple Constant Multiplications. , 2011, , .		3
44	Combination of constant matrix multiplication and gate-level approaches for area and power efficient hybrid radix-2 DIT FFT realization. , 2011, , .		6
45	Hardware implementation of a centroid-based localization algorithm for mobile sensor networks. , 2011, , .		3
46	Low Power Multiple-Value Voltage-Mode Look-Up Table for Quaternary Field Programmable Gate Arrays. Journal of Low Power Electronics, 2011, 7, 294-301.	0.6	0
47	Voltage-mode quaternary FPGAs: An evaluation of interconnections. , 2010, , .		0
48	Design of low-complexity and high-speed digital Finite Impulse Response filters. , 2010, , .		1
49	Radix-2 Decimation in Time (DIT) FFT implementation based on a Matrix-Multiple Constant multiplication approach. , 2010, , .		5
50	Analysis of the conditions for worst case switching activity in integrated circuits. , 2010, , .		0
51	CentroidM. , 2010, , .		9
52	A new quaternary FPGA based on a voltage-mode multi-valued circuit. , 2010, , .		7
53	Optimization of Area and Delay at Gate-Level in Multiple Constant Multiplications. , 2010, , .		9
54	Analysis of Power Consumption Using a New Methodology for the Capacitance Modeling of Complex Logic Gates. Lecture Notes in Computer Science, 2010, , 297-306.	1.3	1

#	Article	IF	Citations
55	Efficient Dedicated Multiplication Blocks for 2Â´s Complement Radix-2m Array Multipliers. Journal of Computers, 2010, 5, .	0.4	10
56	Selected Articles from the PATMOS 2009 Workshop. Journal of Low Power Electronics, 2010, 6, 160-160.	0.6	0
57	Power and delay comparison of binary and quaternary arithmetic circuits. , 2009, , .		5
58	Observability-based coverage-directed path search using PBO for automatic test vector generation. , 2009, , .		1
59	Power macro-modelling using an iterative LS-SVM method. , 2009, , .		0
60	Parameter tuning in SVM-based power macro-modeling. , 2009, , .		2
61	Generating Worst-Case Stimuli for Accurate Power Grid Analysis. Lecture Notes in Computer Science, 2009, , 247-257.	1.3	8
62	Exact and Approximate Algorithms for the Optimization of Area and Delay in Multiple Constant Multiplications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1013-1026.	2.7	92
63	Efficient dedicated multiplication blocks for 2’s complement radix-16 and radix-256 array multipliers. , 2008, , .		5
64	Minimum number of operations under a general number representation for digital filter synthesis. , 2007, , .		7
65	Effect of Number Representation on the Achievable Minimum Number of Operations in Multiple Constant Multiplications. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2007, , .	0.0	8
66	Optimization of Area in Digital FIR Filters using Gate-Level Metrics. Proceedings - Design Automation Conference, 2007, , .	0.0	11
67	A new array architecture for signed multiplication using Gray encoded radix-2moperands. The Integration VLSI Journal, 2007, 40, 118-132.	2.1	3
68	ASSUMEs: Heuristic Algorithms for Optimization of Area and Delay in Digital Filter Synthesis. , 2006, , .		1
69	Optimization of area under a delay constraint in digital filter synthesis using SAT-based integer linear programming. , 2006, , .		2
70	Exploiting general coefficient representation for the optimal sharing of partial products in MCMs. , 2006, , .		4
71	Optimization of area under a delay constraint in digital filter synthesis using SAT-based integer linear programming. Proceedings - Design Automation Conference, 2006, , .	0.0	1
72	Gray Encoded Arithmetic Operators Applied to FFT and FIR Dedicated Datapaths. International Federation for Information Processing, 2006, , 281-297.	0.4	3

#	Article	IF	Citations
73	Design of a Radix-2m Hybrid Array Multiplier Using Carry Save Adder. , 2005, , .		6
74	Performance evaluation of parallel FIR filter optimizations in ASICs and FPGA. , 2005, , .		8
75	Power Estimation Using Probability Polynomials. Design Automation for Embedded Systems, 2004, 9, 19-52.	1.0	3
76	Implicit FSM decomposition applied to low-power design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 560-565.	3.1	21
77	FSM decomposition by direct circuit manipulation applied to low power design. , 2000, , .		7
78	Integrating Dynamic Power Management in the Design Flow. IFIP Advances in Information and Communication Technology, 2000, , 233-244.	0.7	0
79	Assignment and reordering of incompletely specified pattern sequences targetting minimum power dissipation. , 1999, , .		38
80	Sequential logic optimization for low power using input-disabling precomputation architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1998, 17, 279-284.	2.7	20
81	Power Estimation Under User-Specified Input Sequences and Programs. Integrated Computer-Aided Engineering, 1998, 5, 177-185.	4.6	0
82	Estimation of average switching activity in combinational logic circuits using symbolic simulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1997, 16, 121-127.	2.7	68
83	Computer-Aided Design Techniques for Low Power Sequential Logic Circuits. , 1997, , .		21
84	High-Level Power Estimation and Optimization. , 1997, , 151-171.		0
85	Retiming for Low Power. , 1997, , 97-110.		0
86	Power Estimation for Sequential Circuits. , 1997, , 35-80.		0
87	Precomputation. , 1997, , 111-150.		0
88	Techniques for power estimation and optimization at the logic level: A survey. Journal of Signal Processing Systems, 1996, 13, 259-276.	1.0	3
89	RETIMING SEQUENTIAL CIRCUITS FOR LOW POWER. International Journal of High Speed Electronics and Systems, 1996, 07, 323-340.	0.7	3
90	Scheduling techniques to enable power management. , 1996, , .		59

#	Article	IF	Citations
91	Techniques for Power Estimation and Optimization at the Logic Level: A Survey. , 1996, , 175-192.		0
92	Techniques for the power estimation of sequential logic circuits under user-specified input sequences and programs. , 1995, , .		28
93	Power estimation methods for sequential logic circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 1995, 3, 404-416.	3.1	100
94	A methodology for efficient estimation of switching activity in sequential logic circuits. , 1994, , .		73
95	Precomputation-based sequential logic optimization for low power. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 1994, 2, 426-436.	3.1	265
96	Precomputation-based Sequential Logic Optimization For Low Power. , 0, , .		1
97	Retiming sequential circuits for low power. , 0, , .		93
98	Bitwise encoding of finite state machines. , 0, , .		4
99	Optimization of combinational and sequential logic circuits for low power using precomputation. , 0, , .		20
100	Scheduling techniques to enable power management. , 0, , .		27
101	Power optimization of combinational modules using self-timed precomputation. , 0, , .		4
102	Power optimized Viterbi decoder implementation through architectural transforms. , 0, , .		1
103	Power efficient arithmetic operand encoding [CMOS circuits]. , 0, , .		7
104	A new architecture for signed radix-2/sup m/ pure array multipliers. , 0, , .		14
105	A new architecture for 2's complement Gray encoded array multiplier. , 0, , .		7
106	A new pipelined array architecture for signed multiplication. , 0, , .		1
107	Low power architectures for FFT and FIR dedicated datapaths. , 0, , .		1
108	Array hybrid multiplier versus modified booth multiplier: comparing area and power consumption of layout implementations of signed radix-4 architectures. , 0, , .		1

#	Article	IF	Citations
109	Maximal sharing of partial terms in MCM under minimal signed digit representation. , 0, , .		6
110	An exact algorithm for the maximal sharing of partial terms in multiple constant multiplications. , 0, , .		28