Eduardo

List of Publications by Year
in descending order

21 papers	264 citations	1163117 8 h-index	940533 16 g-index
21 all docs	21 docs citations	21 times ranked	136 citing authors

#	Article	IF	Citations
1	Power-Efficient Sum of Absolute Differences Hardware Architecture Using Adder Compressors for Integer Motion Estimation Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 3126-3137.	5.4	53
2	Design Methodology to Explore Hybrid Approximate Adders for Energy-Efficient Image and Video Processing Accelerators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2137-2150.	5.4	52
3	A Cross-Layer Gate-Level-to-Application Co-Simulation for Design Space Exploration of Approximate Circuits in HEVC Video Encoders. IEEE Transactions on Circuits and Systems for Video Technology, 2020, 30, 3814-3828.	8.3	29
4	Approximate Pruned and Truncated Haar Discrete Wavelet Transform VLSI Hardware for Energy-Efficient ECG Signal Processing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1814-1826.	5.4	27
5	Power-, Area-, and Compression-Efficient Eight-Point Approximate 2-D Discrete Tchebichef Transform Hardware Design Combining Truncation Pruning and Efficient Transposition Buffers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 680-693.	5.4	20
6	On the Resiliency of NCFET Circuits Against Voltage Over-Scaling. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1481-1492.	5.4	16
7	Synthesis of High-Order Continuously Tunable Low-Pass Active-R Filters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1841-1854.	5.4	11
8	Fixed-Point NLMS and IPNLMS VLSI Architectures for Accurate FECG and FHR Processing. IEEE Transactions on Biomedical Circuits and Systems, 2021, 15, 898-911.	4.0	11
9	A novel pruned-based algorithm for energy-efficient SATD operation in the HEVC coding. , 2016, , .		7
10	Bridging the Gap Between Voltage Over-Scaling and Joint Hardware Accelerator-Algorithm Closed-Loop. IEEE Transactions on Circuits and Systems for Video Technology, 2022, 32, 398-410.	8.3	6
11	Evaluating the use of adder compressors for power-efficient HEVC interpolation filter architecture. Analog Integrated Circuits and Signal Processing, 2016, 89, 111-120.	1.4	5
12	An Energy-Efficient and Approximate Accelerator Design for Real-Time Canny Edge Detection. Circuits, Systems, and Signal Processing, 2020, 39, 6098-6120.	2.0	5
13	Efficient use of gain-bandwidth product in active filters: Gm-C and Active-R alternatives. , 2017, , .		4
14	A Configurable Pruning Gaussian Image Filter for Energy-Efficient Edge Detection. , 2019, , .		4
15	Design of area and energy-efficient digital CMOS FIR filters with approximate adder circuits. Analog Integrated Circuits and Signal Processing, 2016, 89, 99-109.	1.4	3
16	Exploring approximations in 4- and 8- point DTT hardware architectures for low-power image compression. Analog Integrated Circuits and Signal Processing, 2018, 97, 503-514.	1.4	3
17	Architectural Exploration for Energy-Efficient Fixed-Point Kalman Filter VLSI Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1402-1415.	3.1	3
18	Framework-based Arithmetic Datapath Generation to Explore Parallel Binary Multipliers. Journal of Integrated Circuits and Systems, 2020, 15, 1-10.	0.4	3

#	Article	IF	Citations
19	The 4-2 Fused Adderâ€“Subtractor Compressor for Low-Power Butterfly-Based Hardware Architectures. Circuits, Systems, and Signal Processing, 0, , 1.	2.0	1
20	Design of a low power and robust VLSI power line interference canceler with optimized arithmetic operators. Analog Integrated Circuits and Signal Processing, 2022, 112, 247-261.	1.4	1
21	Exploring the CORDIC Algorithm and Clock-Gating for Power-Efficient Fast Fourier Transform Hardware Architectures. Journal of Integrated Circuits and Systems, 2021, 16, 1-11.	0.4	0