Deog-Kyoon Jeong

List of Publications by Citations

156 papers	2,083 citations	25 h-index	39 g-index
199 ext. papers	2,802 ext. citations	3.8 avg, IF	4.88 L-index

#	Paper	IF	Citations
156	An efficient charge recovery logic circuit. *IEEE Journal of Solid-State Circuits*, **1996**, 31, 514-522	5.5	260
155	An all-analog multiphase delay-locked loop using a replica delay line for wide-range operation and low-jitter performance. *IEEE Journal of Solid-State Circuits*, **2000**, 35, 377-384	5.5	111
154	A 0.18-/spl mu/m CMOS 3.5-gb/s continuous-time adaptive cable equalizer using enhanced low-frequency gain control method. *IEEE Journal of Solid-State Circuits*, **2004**, 39, 419-425	5.5	80
153	Low-voltage high-performance silicon photonic devices and photonic integrated circuits operating up to 30 Gb/s. *Optics Express*, **2011**, 19, 26936-47	3.3	73
152	A Reconfigurable 40-to-67 dB SNR, 50-to-6400 Hz Frame-Rate, Column-Parallel Readout IC for Capacitive Touch-Screen Panels. *IEEE Journal of Solid-State Circuits*, **2014**, 49, 2305-2318	5.5	69
151	A 960-Mb/s/pin interface for skew-tolerant bus using low jitter PLL. *IEEE Journal of Solid-State Circuits*, **1997**, 32, 691-700	5.5	69
150	A fully integrated CMOS frequency synthesizer with charge-averaging charge pump and dual-path loop filter for PCS- and cellular-CDMA wireless systems. *IEEE Journal of Solid-State Circuits*, **2002**, 37, 536-542	5.5	51
149	A 1.0–4.0-Gb/s All-Digital CDR With 1.0-ps Period Resolution DCO and Adaptive Proportional Gain Control. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 424-434	5.5	46
148	Layout Synthesis and Loop Parameter Optimization of a Low-Jitter All-Digital Pixel Clock Generator. *IEEE Journal of Solid-State Circuits*, **2014**, 49, 657-672	5.5	45
147	Silicon photonic receiver and transmitter operating up to 36 Gb/s for ~1550 nm. *Optics Express*, **2015**, 23, 12232-43	3.3	38
146	. *IEEE Journal of Solid-State Circuits*, **1995**, 30, 353-364	5.5	36
145	A Fully Integrated 0.13- mum CMOS 40-Gb/s Serial Link Transceiver. *IEEE Journal of Solid-State Circuits*, **2009**, 44, 1510-1521	5.5	34
144	Jitter transfer analysis of tracked oversampling techniques for multigigabit clock and data recovery. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2003**, 50, 775-783		33
143	A partially switched-opamp technique for high-speed low-power pipelined analog-to-digital converters. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2006**, 53, 795-801		32
142	A 20-GHz phase-locked loop for 40-gb/s serializing transmitter in 0.13-/spl mu/m CMOS. *IEEE Journal of Solid-State Circuits*, **2006**, 41, 899-908	5.5	32
141	Full-CMOS 2-GHz WCDMA direct conversion transmitter and receiver. *IEEE Journal of Solid-State Circuits*, **2003**, 38, 43-53	5.5	32
140	An AC–DC LED Driver With a Two-Parallel Inverted Buck Topology for Reducing the Light Flicker in Lighting Applications to Low-Risk Levels. *IEEE Transactions on Power Electronics*, **2017**, 32, 3879-3891	7.2	31

139	A 5-Gb/s 0.25-/spl mu/m CMOS jitter-tolerant variable-interval oversampling clock/data recovery circuit. *IEEE Journal of Solid-State Circuits*, **2002**, 37, 1822-1830	5.5	31
138	Comprehensive Writing Margin Analysis and its Application to Stacked one Diode-One Memory Device for High-Density Crossbar Resistance Switching Random Access Memory. *Advanced Electronic Materials*, **2016**, 2, 1600326	6.4	31
137	Reducing Ground-Bounce Noise and Stabilizing the Data-Retention Voltage of Power-Gating Structures. *IEEE Transactions on Electron Devices*, **2008**, 55, 197-205	2.9	30
136	A multi-level multi-phase charge-recycling method for low-power AMLCD column drivers. *IEEE Journal of Solid-State Circuits*, **2000**, 35, 74-84	5.5	30
135	Multi-gigabit-rate clock and data recovery based on blind oversampling **2003**, 41, 68-74		29
134	A 22 to 26.5 Gb/s Optical Receiver With All-Digital Clock and Data Recovery in a 65 nm CMOS Process. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 2603-2612	5.5	28
133	A 7.6 mW, 414 fs RMS-Jitter 10 GHz Phase-Locked Loop for a 40 Gb/s Serial Link Transmitter Based on a Two-Stage Ring Oscillator in 65 nm CMOS. *IEEE Journal of Solid-State Circuits*, **2016**, 51, 2357-2367	5.5	28
132	An Optimum Loop Gain Tracking All-Digital PLL Using Autocorrelation of Bang-Bang Phase-Frequency Detection. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2015**, 62, 836-840	3.5	25
131	Design Optimization of On-Chip Inductive Peaking Structures for 0.13-$mu{hbox {m}}$ CMOS 40-Gb/s Transmitter Circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2009**, 56, 2544-2555	3.9	24
130	A single-chip 2.4-GHz direct-conversion CMOS receiver for wireless local loop using multiphase reduced frequency conversion technique. *IEEE Journal of Solid-State Circuits*, **2001**, 36, 800-809	5.5	24
129	A Process-Variation-Tolerant On-Chip CMOS Thermometer for Auto Temperature Compensated Self-Refresh of Low-Power Mobile DRAM. *IEEE Journal of Solid-State Circuits*, **2013**, 48, 2550-2557	5.5	23
128	Comparison frequency doubling and charge pump matching techniques for dual-band /spl Delta//spl Sigma/ fractional-N frequency synthesizer. *IEEE Journal of Solid-State Circuits*, **2005**, 40, 2228-2236	5.5	22
127	A 32/spl times/32-b adiabatic register file with supply clock generator. *IEEE Journal of Solid-State Circuits*, **1998**, 33, 696-701	5.5	21
126	A High-Speed Range-Matching TCAM for Storage-Efficient Packet Classification. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2009**, 56, 1221-1230	3.9	20
125	A crossbar resistance switching memory readout scheme with sneak current cancellation based on a two-port current-mode sensing. *Nanotechnology*, **2016**, 27, 485201	3.4	19
124	A 0.6-2.5-GBaud CMOS tracked 3 /spl times/ oversampling transceiver with dead-zone phase detection for robust clock/data recovery. *IEEE Journal of Solid-State Circuits*, **2001**, 36, 1974-1983	5.5	19
123	A 0.3-1.4 GHz All-Digital Fractional-N PLL With Adaptive Loop Gain Controller. *IEEE Journal of Solid-State Circuits*, **2010**,	5.5	18
122	. *IEEE Journal of Solid-State Circuits*, **1993**, 28, 1350-1353	5.5	18

121	A 0.5-V Fully Synthesizable SAR ADC for On-Chip Distributed Waveform Monitors. *IEEE Access*, **2019**, 7, 63686-63697	3.5	17
120	A 2.5-10-Gb/s CMOS transceiver with alternating edge-sampling phase detection for loop characteristic stabilization. *IEEE Journal of Solid-State Circuits*, **2003**, 38, 1821-1829	5.5	17
119	. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 2982-2993	5.5	17
118	A 2.5–3.6 GHz Subharmonically Injection-Locked All-Digital PLL With Dual-Edge Complementary Switched Injection. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 2691-2702	3.9	16
117	An AC-powered, flicker-free, multi-channel LED driver with current-balancing SIMO buck topology for large area lighting applications **2014**,		16
116	A 0.015-mm$^{text{2}}$ Inductorless 32-GHz Clock Generator With Wide Frequency-Tuning Range in 28-nm CMOS Technology. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 655-659	3.5	15
115	A Mutual Capacitance Touch Readout IC With 64% Reduced-Power Adiabatic Driving Over Heavily Coupled Touch Screen. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 1694-1704	5.5	15
114	A 0.36 pJ/bit, 0.025 mm${}^{text{2}}$, 12.5 Gb/s Forwarded-Clock Receiver With a Stuck-Free Delay-Locked Loop and a Half-Bit Delay Line in 65-nm CMOS Technology. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2016**, 63, 1393-1403	3.9	15
113	A 2.4-GHz 0.25-/spl mu/m CMOS dual-mode direct-conversion transceiver for bluetooth and 802.11b. *IEEE Journal of Solid-State Circuits*, **2004**, 39, 1185-1190	5.5	14
112	A 0.4-to-1 V Voltage Scalable $Delta Sigma $ ADC With Two-Step Hybrid Integrator for IoT Sensor Applications in 65-nm LP CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 1417-1421	3.5	13
111	Review of CMOS Integrated Circuit Technologies for High-Speed Photo-Detection. *Sensors*, **2017**, 17,	3.8	12
110	A Noise-Immunity-Enhanced Analog Front-End for $36times64$ Touch-Screen Controllers With 20-$text{V}_{text{PP}}$ Noise Tolerance at 100 kHz. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 1497-1510	5.5	11
109	A 0.1-pJ/b/dB 1.62-to-10.8-Gb/s Video Interface Receiver With Jointly Adaptive CTLE and DFE Using Biased Data-Level Reference. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 2186-2195	5.5	10
108	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 2234-2243	2.6	10
107	250 Mbps–3 Gbps Wide-Range CDR With Digital Vernier Phase Shifting and Dual-Mode Control in 0.13 mum CMOS. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 2560-2570	5.5	10
106	A 1.2-V-only 900-mW 10 gb ethernet transceiver and XAUI interface with robust VCO tuning technique. *IEEE Journal of Solid-State Circuits*, **2005**, 40, 2148-2158	5.5	10
105	A 20 Gb/s 0.4 pJ/b Energy-Efficient Transmitter Driver Utilizing Constant- ${rm G}_{rm m}$ Bias. *IEEE Journal of Solid-State Circuits*, **2016**, 51, 2312-2327	5.5	10
104	6.5 A 6.4-to-32Gb/s 0.96pJ/b Referenceless CDR Employing ML-Inspired Stochastic Phase-Frequency Detection Technique in 40nm CMOS **2020**,		9

103	A Supply-Scalable-Serializing Transmitter With Controllable Output Swing and Equalization for Next-Generation Standards. *IEEE Transactions on Industrial Electronics*, **2017**, 1-1	8.9	9
102	A 0.25-mum CMOS 1.9-GHz PHS RF Transceiver With a 150-kHz Low-IF Architecture. *IEEE Journal of Solid-State Circuits*, **2007**, 42, 1318-1327	5.5	9
101	A Single-Pair Serial Link for Mobile Displays With Clock Edge Modulation Scheme. *IEEE Journal of Solid-State Circuits*, **2007**, 42, 2012-2020	5.5	9
100	A quad 0.6-3.2 Gb/s/channel interference-free CMOS transceiver for backplane serial link. *IEEE Journal of Solid-State Circuits*, **2004**, 39, 795-803	5.5	9
99	A 2-Gbaud 0.7-V swing voltage-mode driver and on-chip terminator for high-speed NRZ data transmission. *IEEE Journal of Solid-State Circuits*, **2000**, 35, 915-918	5.5	9
98	A 2.44-pJ/b 1.62□10-Gb/s Receiver for Next Generation Video Interface Equalizing 23-dB Loss With Adaptive 2-Tap Data DFE and 1-Tap Edge DFE. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1295-1299	3.5	9
97	A 180-Mb/s to 3.2-Gb/s, continuous-rate, fast-locking CDR without using external reference clock **2007**,		8
96	A 2.8Gb/s All-Digital CDR with a 10b Monotonic DCO **2007**,		8
95	An Optimum Injection-Timing Tracking Loop for 5-GHz, 1.13-mW/GHz RO-Based Injection-Locked PLL With 152-fs Integrated Jitter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1819-1823	3.5	8
94	A 5-GHz subharmonically injection-locked all-digital PLL with complementary switched injection **2015**,		7
93	A 1-pJ/bit, 10-Gb/s/ch Forwarded-Clock Transmitter Using a Resistive Feedback Inverter-Based Driver in 65-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2016**, 63, 1106-1110	3.5	7
92	Real-Time External Compensation of Threshold Voltage Shift Using Double-Gate Oxide TFTs in a Gate Driving System. *Journal of Display Technology*, **2016**, 12, 892-897		7
91	A Four-Channel 32-Gb/s Transceiver With Current-Recycling Output Driver and On-Chip AC Coupling in 65-nm CMOS Process. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2014**, 61, 304-308	3.5	7
90	A low-noise differential front-end and its controller for capacitive touch screen panels **2012**,		7
89	A Fast-Locking CDR Circuit with an Autonomously Reconfigurable Charge Pump and Loop Filter **2006**,		7
88	Clock dithering for electromagnetic compliance using spread spectrum phase modulation		7
87	A 4□0-Gb/s 1.87-pJ/b Continuous-Rate Digital CDR Circuit With Unlimited Frequency Acquisition Capability in 65-nm CMOS. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 1597-1607	5.5	7
86	A 0.6-to-1V 10k-to-100kHz BW 11.7b-ENOB Noise-Shaping SAR ADC for IoT sensor applications in 28-nm CMOS **2018**,		7

85	A 32 Gb/s, 201 mW, MZM/EAM Cascode Push-Pull CML Driver in 65 nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 436-440	3.5	6
84	A 20-Gb/s 1.27pJ/b low-power optical receiver front-end in 65nm CMOS **2014**,		6
83	1.04 GBd low EMI digital video interface system using small swing serial link technique. *IEEE Journal of Solid-State Circuits*, **1998**, 33, 816-823	5.5	6
82	Efficient charge recovery logic		6
81	Ultra-low-voltage low-power dynamic comparator with forward body bias scheme for SAR ADC. *Electronics Letters*, **2018**, 54, 1370-1372	1.1	6
80	Reference Spur Reduction Techniques for a Phase-Locked Loop. *IEEE Access*, **2019**, 7, 38035-38043	3.5	5
79	A power-efficient 600-mVpp voltage-mode driver with independently matched pull-up and pull-down impedances. *International Journal of Circuit Theory and Applications*, **2015**, 43, 2057-2071	2	5
78	. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1894-1898	3.5	5
77	A 27.1 mW, 7.5-to-11.1 Gb/s single-loop referenceless CDR with direct Up/dn control **2017**,		5
76	A 28 Gb/s 1.6 pJ/b PAM-4 Transmitter Using Fractionally Spaced 3-Tap FFE and G_{m} -Regulated Resistive-Feedback Driver. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 1377-1381	3.5	5
75	A 0.36 pJ/bit, 12.5 Gb/s forwarded-clock receiver with a sample swapping scheme and a half-bit delay line **2014**,		5
74	A spread spectrum clock generation PLL with dual-tone modulation profile		5
73	A CMOS 3.5 Gbps continuous-time adaptive cable equalizer with joint adaptation method of low-frequency gain and high-frequency boosting		5
72	A Fast Droop-Recovery Event-Driven Digital LDO With Adaptive Linear/Binary Two-Step Search for Voltage Regulation in Advanced Memory. *IEEE Transactions on Power Electronics*, **2021**, 1-1	7.2	5
71	A 20 k-to-100kS/s Sub- mu W 9.5b-ENOB Asynchronous SAR ADC for Energy-Harvesting Body Sensor Node SoCs in 0.18- mu m CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1814-1818	3.5	5
70	Adiabatically driven touch controller analog front-end for ultra-thin displays **2018**,		4
69	1.2 V 10-bit 75 MS/s Pipelined ADC With Phase-Dependent Gain-Transition CDS. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 585-592	2.6	4
68	A single-inductor, multiple-channel current-balancing LED driver for display backlight applications **2013**,		4

67	A 15-GHz, 17.8-mW, 213-fs Injection-Locked PLL With Maximized Injection Strength Using Adjustment of Phase Domain Response. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 1932-1936	3.5	4
66	A Fully Integrated 700mA Event-Driven Digital Low-Dropout Regulator with Residue-Tracking Loop for Fine-Grained Power Management Unit **2018**,		4
65	A 4-to-20Gb/s 1.87pJ/b Referenceless Digital CDR With Unlimited Frequency Detection Capability in 65nm CMOS **2019**,		3
64	A 10 Gb/s hybrid PLL-based forwarded clock receiver in 65-nm CMOS **2015**,		3
63	A Highly Synthesizable 0.5-to-1.0-V Digital Low-Dropout Regulator With Adaptive Clocking and Incremental Regulation Scheme. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 2174-2178	3.5	3
62	A 55.1 mW 1.62-to-8.1 Gb/s Video Interface Receiver Generating up to 680 MHz Stream Clock Over 20 dB Loss Channel. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 1432-1436	3.5	3
61	A Modulo-FIR Equalizer for Wireline Communications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 4278-4286	3.9	3
60	4-Slot, 8-Drop Impedance-Matched Bidirectional Multidrop DQ Bus With a 4.8-Gb/s Memory Controller Transceiver. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2013**, 3, 858-869	1.7	3
59	A compact 87.1-dB DR bandwidth-scalable delta-sigma modulator based on dynamic gain-bandwidth-boosting inverter for audio applications **2017**,		3
58	A single-chip 2.4 GHz direct-conversion CMOS transceiver with GFSK modem for Bluetooth application		3
57	An Adaptive Offset Cancellation Scheme and Shared-Summer Adaptive DFE for 0.068 pJ/b/dB 1.62-to-10 Gb/s Low-Power Receiver in 40 nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 622-626	3.5	3
56	Real-time current-sensing feedback system for compensating process□oltage□emperature variations of display using double-gate oxide TFT. *Electronics Letters*, **2017**, 53, 117-119	1.1	2
55	A 2.5□8 Gb/s Multi-Standard Transmitter With Two-Step Time-Multiplexing Driver. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 1927-1931	3.5	2
54	A 370-fJ/b, 0.0056 mm2/DQ, 4.8-Gb/s DQ Receiver for HBM3 with a Baud-Rate Self-Tracking Loop **2019**,		2
53	32.4 A 0.4-to-1.2V 0.0057mm2 55fs-Transient-FoM Ring-Amplifier-Based Low-Dropout Regulator with Replica-Based PSR Enhancement **2020**,		2
52	Design of Soft-Switching Hybrid DC-DC Converter with 2-Phase Switched Capacitor and 0.8nH Inductor for Standard CMOS Process. *Electronics (Switzerland)*, **2020**, 9, 372	2.6	2
51	A Capacitor-Coupled Offset-Canceled Sense Amplifier for DRAMs With Reduced Variation of Decision Threshold Voltage. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 2219-2227	5.5	2
50	Analysis of frequency detection capability of Alexander phase detector. *Electronics Letters*, **2020**, 56, 180-182	1.1	2

49	A 64Gb/s 2.29pJ/b PAM-4 VCSEL Transmitter With 3-Tap Asymmetric FFE in 65nm CMOS **2019**,		2
48	A 10-Gb/s 6-Vpp differential modulator driver in 65-nm CMOS **2014**,		2
47	A 20 Gb/s 0.4 pJ/b energy-efficient transmitter driver architecture utilizing constant Gm **2015**,		2
46	Use of Phase Delay Analysis for Evaluating Wideband Circuits: An Alternative to Group Delay Analysis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 3543-3547	2.6	2
45	A 7.6 mW, 214-fs RMS jitter 10-GHz phase-locked loop for 40-Gb/s serial link transmitter based on two-stage ring oscillator in 65-nm CMOS **2015**,		2
44	A PVT-insensitive time-to-digital converter using fractional difference Vernier delay lines **2009**,		2
43	A 20-Gb/s full-rate 27-1 PRBS generator integrated with 20-GHz PLL in 0.13-μm CMOS **2008**,		2
42	An 8-bit 125 MS/s CMOS folding ADC for Gigabit Ethernet LSI		2
41	A 285-fsrmsIntegrated Jitter Injection-Locked Ring PLL with Charge-Stored Complementary Switch Injection Technique. *Journal of Semiconductor Technology and Science*, **2016**, 16, 860-866	1.5	2
40	A Maximum-Eye-Tracking CDR With Biased Data-Level and Eye Slope Detector for Near-Optimal Timing Adaptation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 2708-2720	2.6	2
39	25-Gb/s Clocked Pluggable Optics for High-Density Data Center Interconnections. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1395-1399	3.5	2
38	A PVT Variation-Robust All-Digital Injection-Locked Clock Multiplier With Real-Time Offset Tracking Using Time-Division Dual Calibration. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 2525-2538	5.5	2
37	25 Gb/s photoreceiver based on vertical-illumination type Ge-on-Si photodetector and CMOS amplifier circuit for optical interconnects **2015**,		1
36	A low-power pulse position modulation transceiver **2015**,		1
35	A 48 Gb/s PAM-4 Transmitter With 3-Tap FFE Based on Double-Shielded Coplanar Waveguide in 65-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 1569-1573	3.5	1
34	A 22-Gb/s 0.95-pJ/b Energy-Efficient Voltage-Mode Transmitter With Time-Based Feedforward Equalization in a 28-nm CMOS. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1099-1106	2.6	1
33	A 10-Gb/s, 0.03-mm2, 1.28-pJ/bit Half-Rate Injection-Locked CDR With Path Mismatch Tracking Loop in a 28-nm CMOS Technology. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 2812-2822	5.5	1
32	A compact 22-Gb/s transmitter for optical links with all-digital phase-locked loop **2015**,		1

31	58.4: 10-Bit Column Driver with Split-DAC Architecture. *Digest of Technical Papers SID International Symposium*, **2008**, 39, 892	0.5	1
30	A Bandpass Interface IC for Sacrificial Bulk Micromachined Inertial Sensors **2006**,		1
29	An 1.4Gbps/ch LVDS Receiver with Jitter-Boundary-Based Digital De-skew Algorithm **2006**,		1
28	A 3-mW, 270-Mbps, Clock-Edge Modulated Serial Link for Mobile Displays **2005**,		1
27	A 62.5-250 MHz multi-phase delay-locked loop using a replica delay line with triply controlled delay cells		1
26	Design Techniques for a 6.4-32-Gb/s 0.96-pJ/b Continuous-Rate CDR With Stochastic Frequency-Phase Detector. *IEEE Journal of Solid-State Circuits*, **2021**, 1-1	5.5	1
25	A 500 MHz-to-1.2 GHz Reset Free Delay Locked Loop for Memory Controller with Hysteresis Coarse Lock Detector. *Journal of Semiconductor Technology and Science*, **2011**, 11, 73-79	1.5	1
24	A 0.45 pJ/b, 6.4 Gb/s Forwarded-Clock Receiver With DLL-Based Self-Tracking Loop for Unmatched Memory Interfaces. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 1814-1818	3.5	1
23	A Programmable On-Chip Reference Oscillator With Slow-Wave Coplanar Waveguide in 14-nm FinFET CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 1834-1838	3.5	1
22	An Always-On 0.53-to-13.4 mW Power-Scalable Touchscreen Controller for Ultrathin Touchscreen Displays With Current-Mode Filter and Incremental Hybrid ADC **2019**,		1
21	A 10-Gb/s, 0.03-mm2, 1.28-pJ/bit Half-Rate All-Digital Injection-Locked Clock and Data Recovery with Maximum Timing-Margin Tracking Loop **2018**,		1
20	A Crystal-Less Programmable Clock Generator with RC-LC Hybrid Oscillator for GHz Applications in 14 nm FinFET CMOS **2018**,		1
19	A 1.93-pJ/Bit PCI Express Gen4 PHY Transmitter with On-Chip Supply Regulators in 28 nm CMOS. *Electronics (Switzerland)*, **2021**, 10, 68	2.6	1
18	A Residue-Current-Locked Hybrid Low-Dropout Regulator Supporting Ultralow Dropout of Sub-50 mV With Fast Settling Time Below 10 ns. *IEEE Journal of Solid-State Circuits*, **2021**, 1-1	5.5	0
17	A 10 Gb/s PAM-4 Transmitter With Feed-Forward Implementation of Tomlinson-Harashima Precoding in 28 nm CMOS. *IEEE Access*, **2021**, 1-1	3.5	0
16	A Combined Clock and Data Recovery Circuit with Adaptive Cancellation of Data-Dependent Jitter. *Journal of Semiconductor Technology and Science*, **2008**, 8, 193-199	1.5	0
15	A 0.83-pJ/Bit 6.4-Gb/s HBM Base Die Receiver Using a 45 Strobe Phase for Energy-Efficient Skew Compensation. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 1735-1739	3.5	0
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13	A 35-Gb/s 0.65-pJ/b Asymmetric Push-Pull Inverter-Based VCSEL Driver With Series Inductive Peaking in 65-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1824-1828	3.5	0
12	Design of High Step-Down Ratio Isolated Three-Level Half-Bridge DC-DC Converter with Balanced Voltage on Flying Capacitor. *IEEE Transactions on Power Electronics*, **2022**, 1-1	7.2	0
11	A 2.5 -32 Gb/s Gen 5-PCIe Receiver with Multi-Rate CDR Engine and Hybrid DFE. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2022**, 1-1	3.5	0
10	27.3: 1.2 Gbps GDDR3 Physical Layer for 3D AMOLED Panel. *Digest of Technical Papers SID International Symposium*, **2011**, 42, 357-360	0.5	
9	Area and Power Efficient 10B6Q PAM-4 DC Balance Coder for Automotive Camera Link. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2022**, 1-1	3.5	
8	An 8-GHz Octa-Phase Error Corrector with Coprime Phase Comparison Scheme in 40-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 1-1	3.5	
7	A 1.05-to-3.2GHz All-Digital PLL for DDR5 Registering Clock Driver with a Self-Biased Supply-Noise-Compensating Ring DCO. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 1-1	3.5	
6	Balancing scheme for phase current and flying-capacitor voltage in three-level DC–DC converter. *Electronics Letters*, **2020**, 56, 426-428	1.1	
5	Synthesisable glitch-less phase rotator with conditionally cascading scheme. *Electronics Letters*, **2020**, 56, 536-538	1.1	
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