Deog-Kyoon Jeong

List of Publications by Year
in descending order

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199 papers	3,334 citations	172207 29 h-index	197535 49 g-index
199 all docs	199 docs citations	199 times ranked	2022 citing authors

#	Article	IF	Citations
1	An efficient charge recovery logic circuit. IEEE Journal of Solid-State Circuits, 1996, 31, 514-522.	3.5	411
2	An all-analog multiphase delay-locked loop using a replica delay line for wide-range operation and low-jitter performance. IEEE Journal of Solid-State Circuits, 2000, 35, 377-384.	3.5	156
3	A Reconfigurable 40-to-67 dB SNR, 50-to-6400 Hz Frame-Rate, Column-Parallel Readout IC for Capacitive Touch-Screen Panels. IEEE Journal of Solid-State Circuits, 2014, 49, 2305-2318.	3.5	117
4	Low-voltage high-performance silicon photonic devices and photonic integrated circuits operating up to 30 Gb/s. Optics Express, 2011, 19, 26936.	1.7	111
5	A 0.18-<tex>$muhboxm$</tex>CMOS 3.5-Gb/s Continuous-Time Adaptive Cable Equalizer Using Enhanced Low-Frequency Gain Control Method. IEEE Journal of Solid-State Circuits, 2004, 39, 419-425.	3.5	109
6	A 960-Mb/s/pin interface for skew-tolerant bus using low jitter PLL. IEEE Journal of Solid-State Circuits, 1997, 32, 691-700.	3.5	102
7	Silicon photonic receiver and transmitter operating up to 36 Gb/s for Î»~1550 nm. Optics Express, 2015, 23, 12232.	1.7	77
8	Layout Synthesis and Loop Parameter Optimization of a Low-Jitter All-Digital Pixel Clock Generator. IEEE Journal of Solid-State Circuits, 2014, 49, 657-672.	3.5	73
9	A fully integrated CMOS frequency synthesizer with charge-averaging charge pump and dual-path loop filter for PCS- and cellular-CDMA wireless systems. IEEE Journal of Solid-State Circuits, 2002, 37, 536-542.	3.5	69
10	A CMOS serial link for fully duplexed data communication. IEEE Journal of Solid-State Circuits, 1995, 30, 353-364.	3.5	61
11	A 5-Gb/s 0.25-Î¼m CMOS jitter-tolerant variable-interval oversampling clock/data recovery circuit. IEEE Journal of Solid-State Circuits, 2002, 37, 1822-1830.	3.5	58
12	Multi-gigabit-rate clock and data recovery based on blind oversampling. , 2003, 41, 68-74.		57
13	A 1.0â€“4.0-Gb/s All-Digital CDR With 1.0-ps Period Resolution DCO and Adaptive Proportional Gain Control. IEEE Journal of Solid-State Circuits, 2011, 46, 424-434.	3.5	57
14	Full-CMOS 2-GHz WCDMA direct conversion transmitter and receiver. IEEE Journal of Solid-State Circuits, 2003, 38, 43-53.	3.5	52
15	An ACâ€“DC LED Driver With a Two-Parallel Inverted Buck Topology for Reducing the Light Flicker in Lighting Applications to Low-Risk Levels. IEEE Transactions on Power Electronics, 2017, 32, 3879-3891.	5.4	49
16	Reducing Ground-Bounce Noise and Stabilizing the Data-Retention Voltage of Power-Gating Structures. IEEE Transactions on Electron Devices, 2008, 55, 197-205.	1.6	45
17	A partially switched-opamp technique for high-speed low-power pipelined analog-to-digital converters. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 795-801.	0.1	44
18	Design Optimization of On-Chip Inductive Peaking Structures for 0.13-$mu{hbox {m}}$ CMOS 40-Gb/s Transmitter Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 2544-2555.	3.5	44

#	Article	IF	Citations
19	A 7.6 mW, 414 fs RMS-Jitter 10 GHz Phase-Locked Loop for a 40 Gb/s Serial Link Transmitter Based on a Two-Stage Ring Oscillator in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2016, 51, 2357-2367.	3.5	44
20	A multi-level multi-phase charge-recycling method for low-power AMLCD column drivers. IEEE Journal of Solid-State Circuits, 2000, 35, 74-84.	3.5	42
21	A single-chip 2.4-GHz direct-conversion CMOS receiver for wireless local loop using multiphase reduced frequency conversion technique. IEEE Journal of Solid-State Circuits, 2001, 36, 800-809.	3.5	42
22	A 20-GHz Phase-Locked Loop for 40-Gb/s Serializing Transmitter in 0.13-<tex>$muhboxm$</tex>CMOS. IEEE Journal of Solid-State Circuits, 2006, 41, 899-908.	3.5	42
23	A Fully Integrated 0.13-mum CMOS 40-Gb/s Serial Link Transceiver. IEEE Journal of Solid-State Circuits, 2009, 44, 1510-1521.	3.5	42
24	A 22 to 26.5 Gb/s Optical Receiver With All-Digital Clock and Data Recovery in a 65 nm CMOS Process. IEEE Journal of Solid-State Circuits, 2015, 50, 2603-2612.	3.5	42
25	Jitter transfer analysis of tracked oversampling techniques for multigigabit clock and data recovery. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2003, 50, 775-783.	2.3	40
26	An Optimum Loop Gain Tracking All-Digital PLL Using Autocorrelation of Bangâ€“Bang Phase-Frequency Detection. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 836-840.	2.2	37
27	Comprehensive Writing Margin Analysis and its Application to Stacked one Diodeâ€One Memory Device for Highâ€Density Crossbar Resistance Switching Random Access Memory. Advanced Electronic Materials, 2016, 2, 1600326.	2.6	34
28	A 0.3â€“1.4 GHz All-Digital Fractional-N PLL With Adaptive Loop Gain Controller. IEEE Journal of Solid-State Circuits, 2010, , .	3.5	33
29	A Process-Variation-Tolerant On-Chip CMOS Thermometer for Auto Temperature Compensated Self-Refresh of Low-Power Mobile DRAM. IEEE Journal of Solid-State Circuits, 2013, 48, 2550-2557.	3.5	32
30	Comparison frequency doubling and charge pump matching techniques for dual-band /spl Delta//spl Sigma/ fractional-N frequency synthesizer. IEEE Journal of Solid-State Circuits, 2005, 40, 2228-2236.	3.5	31
31	A 32Ã—32-b adiabatic register file with supply clock generator. IEEE Journal of Solid-State Circuits, 1998, 33, 696-701.	3.5	30
32	A 6.7â€“11.2 Gb/s, 2.25 pJ/bit, Single-Loop Referenceless CDR With Multi-Phase, Oversampling PFD in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 2982-2993.	3.5	30
33	A 0.1-pJ/b/dB 1.62-to-10.8-Gb/s Video Interface Receiver With Jointly Adaptive CTLE and DFE Using Biased Data-Level Reference. IEEE Journal of Solid-State Circuits, 2020, 55, 2186-2195.	3.5	29
34	A 2.4-GHz 0.25-/spl mu/m CMOS dual-mode direct-conversion transceiver for bluetooth and 802.11b. IEEE Journal of Solid-State Circuits, 2004, 39, 1185-1190.	3.5	28
35	A 0.6-2.5-GBaud CMOS tracked 3 Ã— oversampling transceiver with dead-zone phase detection for robust clock/data recovery. IEEE Journal of Solid-State Circuits, 2001, 36, 1974-1983.	3.5	27
36	A 0.5-V Fully Synthesizable SAR ADC for On-Chip Distributed Waveform Monitors. IEEE Access, 2019, 7, 63686-63697.	2.6	27

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37	A 2.5 - 10-Gb/s CMOS transceiver with alternating edge-sampling phase detection for loop characteristic stabilization. IEEE Journal of Solid-State Circuits, 2003, 38, 1821-1829.	3.5	26
38	Class-AB large-swing CMOS buffer amplifier with controlled bias current. IEEE Journal of Solid-State Circuits, 1993, 28, 1350-1353.	3.5	25
39	A High-Speed Range-Matching TCAM for Storage-Efficient Packet Classification. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1221-1230.	3.5	25
40	A crossbar resistance switching memory readout scheme with sneak current cancellation based on a two-port current-mode sensing. Nanotechnology, 2016, 27, 485201.	1.3	24
41	A Mutual Capacitance Touch Readout IC With 64% Reduced-Power Adiabatic Driving Over Heavily Coupled Touch Screen. IEEE Journal of Solid-State Circuits, 2019, 54, 1694-1704.	3.5	24
42	A 4â€“20-Gb/s 1.87-pJ/b Continuous-Rate Digital CDR Circuit With Unlimited Frequency Acquisition Capability in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2021, 56, 1597-1607.	3.5	24
43	A Noise-Immunity-Enhanced Analog Front-End for $36imes64$ Touch-Screen Controllers With 20-$ext{V}_{ext{PP}}$ Noise Tolerance at 100 kHz. IEEE Journal of Solid-State Circuits, 2019, 54, 1497-1510.	3.5	23
44	An AC-powered, flicker-free, multi-channel LED driver with current-balancing SIMO buck topology for large area lighting applications. , 2014, , .		21
45	A 180-Mb/s to 3.2-Gb/s, continuous-rate, fast-locking CDR without using external reference clock. , 2007, , .		19
46	A 0.36 pJ/bit, 0.025 mm<inline-formula> <tex-math notation="LaTeX">${}^{ext{2}}$</tex-math> </inline-formula>, 12.5 Gb/s Forwarded-Clock Receiver With a Stuck-Free Delay-Locked Loop and a Half-Bit Delay Line in 65-nm CMOS Technology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1393-1403.	3.5	19
47	A 2.5â€“5.6 GHz Subharmonically Injection-Locked All-Digital PLL With Dual-Edge Complementary Switched Injection. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 2691-2702.	3.5	19
48	A 0.015-mm<inline-formula> <tex-math notation="LaTeX">$^{ext{2}}$</tex-math> </inline-formula> Inductorless 32-GHz Clock Generator With Wide Frequency-Tuning Range in 28-nm CMOS Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 655-659.	2.2	18
49	6.5 A 6.4-to-32Gb/s 0.96pJ/b Referenceless CDR Employing ML-Inspired Stochastic Phase-Frequency Detection Technique in 40nm CMOS. , 2020, , .		18
50	Efficient charge recovery logic. , 0, , .		16
51	A 0.4-to-1 V Voltage Scalable $Delta Sigma $ ADC With Two-Step Hybrid Integrator for IoT Sensor Applications in 65-nm LP CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1417-1421.	2.2	16
52	Clock dithering for electromagnetic compliance using spread spectrum phase modulation. , 0, , .		15
53	A Single-Pair Serial Link for Mobile Displays With Clock Edge Modulation Scheme. IEEE Journal of Solid-State Circuits, 2007, 42, 2012-2020.	3.5	15
54	A 20 Gb/s 0.4 pJ/b Energy-Efficient Transmitter Driver Utilizing Constant-<inline-formula> <tex-math notation="LaTeX">${m G}_{m m}$ </tex-math> </inline-formula> Bias. IEEE Journal of Solid-State Circuits, 2016, 51, 2312-2327.	3.5	15

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55	Ultraâ€lowâ€voltage lowâ€power dynamic comparator with forward body bias scheme for SAR ADC. Electronics Letters, 2018, 54, 1370-1372.	0.5	15
56	A 2.8Gb/s All-Digital CDR with a 10b Monotonic DCO. , 2007, , .		14
57	A 2.44-pJ/b 1.62â€“10-Gb/s Receiver for Next Generation Video Interface Equalizing 23-dB Loss With Adaptive 2-Tap Data DFE and 1-Tap Edge DFE. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1295-1299.	2.2	14
58	Design of Silicon Photonic Interconnect ICs in 65-nm CMOS Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2234-2243.	2.1	13
59	Review of CMOS Integrated Circuit Technologies for High-Speed Photo-Detection. Sensors, 2017, 17, 1962.	2.1	13
60	A 0.6-to-1V 10k-to-100kHz BW 11.7b-ENOB Noise-Shaping SAR ADC for IoT sensor applications in 28-nm CMOS. , 2018, , .		13
61	A Fast Droop-Recovery Event-Driven Digital LDO With Adaptive Linear/Binary Two-Step Search for Voltage Regulation in Advanced Memory. IEEE Transactions on Power Electronics, 2021, , 1-1.	5.4	13
62	A 2-Gbaud 0.7-V swing voltage-mode driver and on-chip terminator for high-speed NRZ data transmission. IEEE Journal of Solid-State Circuits, 2000, 35, 915-918.	3.5	12
63	A 32 Gb/s, 201 mW, MZM/EAM Cascode Pushâ€“Pull CML Driver in 65 nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 436-440.	2.2	12
64	A quad 0.6-3.2 Gb/s/channel interference-free CMOS transceiver for backplane serial link. IEEE Journal of Solid-State Circuits, 2004, 39, 795-803.	3.5	11
65	A 1.2-V-only 900-mW 10 gb ethernet transceiver and XAUI interface with robust VCO tuning technique. IEEE Journal of Solid-State Circuits, 2005, 40, 2148-2158.	3.5	11
66	250 Mbpsâ€“5 Gbps Wide-Range CDR With Digital Vernier Phase Shifting and Dual-Mode Control in 0.13 mum CMOS. IEEE Journal of Solid-State Circuits, 2011, 46, 2560-2570.	3.5	11
67	A 5-GHz subharmonically injection-locked all-digital PLL with complementary switched injection. , 2015, , .		11
68	Reference Spur Reduction Techniques for a Phase-Locked Loop. IEEE Access, 2019, 7, 38035-38043.	2.6	11
69	A 32 X 32-bit Adiabatic Register File With Supply Clock Generator. , 1997, , .		10
70	1.04 GBd low EMI digital video interface system using small swing serial link technique. IEEE Journal of Solid-State Circuits, 1998, 33, 816-823.	3.5	10
71	A spread spectrum clock generation PLL with dual-tone modulation profile. , 0, , .		10
72	A 0.25-mum CMOS 1.9-GHz PHS RF Transceiver With a 150-kHz Low-IF Architecture. IEEE Journal of Solid-State Circuits, 2007, 42, 1318-1327.	3.5	9

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73	A 20-Gb/s full-rate 2⁷-1 PRBS generator integrated with 20-GHz PLL in 0.13-μm CMOS. , 2008, , .		9
74	A low-noise differential front-end and its controller for capacitive touch screen panels. , 2012, , .		9
75	Real-Time External Compensation of Threshold Voltage Shift Using Double-Gate Oxide TFTs in a Gate Driving System. Journal of Display Technology, 2016, 12, 892-897.	1.3	9
76	A 28 Gb/s 1.6 pJ/b PAM-4 Transmitter Using Fractionally Spaced 3-Tap FFE and G_{m} -Regulated Resistive-Feedback Driver. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1377-1381.	2.2	9
77	A Supply-Scalable Serializing Transmitter with Controllable Output Swing and Equalization for Next Generation Standards. IEEE Transactions on Industrial Electronics, 2017, , 1-1.	5.2	9
78	An Optimum Injection-Timing Tracking Loop for 5-GHz, 1.13-mW/GHz RO-Based Injection-Locked PLL With 152-fs Integrated Jitter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1819-1823.	2.2	9
79	A Capacitor-Coupled Offset-Canceled Sense Amplifier for DRAMs With Reduced Variation of Decision Threshold Voltage. IEEE Journal of Solid-State Circuits, 2020, 55, 2219-2227.	3.5	9
80	A Highly Synthesizable 0.5-to-1.0-V Digital Low-Dropout Regulator With Adaptive Clocking and Incremental Regulation Scheme. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2174-2178.	2.2	9
81	Design Techniques for a 6.4â€“32-Gb/s 0.96-pJ/b Continuous-Rate CDR With Stochastic Frequencyâ€“Phase Detector. IEEE Journal of Solid-State Circuits, 2022, 57, 573-585.	3.5	9
82	A single-chip 2.4 GHz direct-conversion CMOS receiver for wireless local loop using one-third frequency local oscillator. , 0, , .		8
83	A single-chip 2.4 GHz direct-conversion CMOS transceiver with GFSK modem for Bluetooth application. , 0, , .		8
84	A Four-Channel 32-Gb/s Transceiver With Current-Recycling Output Driver and On-Chip AC Coupling in 65-nm CMOS Process. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 304-308.	2.2	8
85	A 20 Gb/s 0.4 pJ/b energy-efficient transmitter driver architecture utilizing constant Gm. , 2015, , .		8
86	A 1-pJ/bit, 10-Gb/s/ch Forwarded-Clock Transmitter Using a Resistive Feedback Inverter-Based Driver in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 1106-1110.	2.2	8
87	A 35-Gb/s 0.65-pJ/b Asymmetric Push-Pull Inverter-Based VCSEL Driver With Series Inductive Peaking in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1824-1828.	2.2	8
88	A 64Gb/s 2.29pJ/b PAM-4 VCSEL Transmitter With 3-Tap Asymmetric FFE in 65nm CMOS. , 2019, , .		8
89	Design of High Step-Down Ratio Isolated Three-Level Half-Bridge DCâ€“DC Converter With Balanced Voltage on Flying Capacitor. IEEE Transactions on Power Electronics, 2022, 37, 10213-10225.	5.4	8
90	A CMOS 3.5 Gbps continuous-time adaptive cable equalizer with joint adaptation method of low-frequency gain and high-frequency boosting. , 0, , .		7

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91	A Fast-Locking CDR Circuit with an Autonomously Reconfigurable Charge Pump and Loop Filter. , 2006, , .		7
92	A 26.5–37.5 GHz frequency divider and a 73-GHz-BW CML buffer in 0.13μm CMOS. , 2007, , .		7
93	A 20-Gb/s 1.27pJ/b low-power optical receiver front-end in 65nm CMOS. , 2014, , .		7
94	A powerâ€efficient 600â€mV_{pp} voltageâ€mode driver with independently matched pullâ€up and pullâ€down impedances. International Journal of Circuit Theory and Applications, 2015, 43, 2057-2071.	1.3	7
95	A 27.1 mW, 7.5-to-11.1 Gb/s single-loop referenceless CDR with direct Up/dn control. , 2017, , .		7
96	A 20 k-to-100kS/s Sub-<inline-formula> <tex-math notation="LaTeX">mu </tex-math> </inline-formula>W 9.5b-ENOB Asynchronous SAR ADC for Energy-Harvesting Body Sensor Node SoCs in 0.18-<inline-formula> <tex-math notation="LaTeX">mu </tex-math> </inline-formula>m CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1814-1818.	2.2	7
97	A 4266 Mb/s/pin LPDDR4 Interface With An Asynchronous Feedback CTLE and An Adaptive 3-Step Eye Detection Algorithm for Memory Controller. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1894-1898.	2.2	7
98	An Adaptive Offset Cancellation Scheme and Shared-Summer Adaptive DFE for 0.068 pJ/b/dB 1.62-to-10 Gb/s Low-Power Receiver in 40 nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 622-626.	2.2	7
99	A 0.36 pJ/bit, 12.5 Gb/s forwarded-clock receiver with a sample swapping scheme and a half-bit delay line. , 2014, , .		6
100	A 10 Gb/s hybrid PLL-based forwarded clock receiver in 65-nm CMOS. , 2015, , .		6
101	A Fully Integrated 700mA Event-Driven Digital Low-Dropout Regulator with Residue-Tracking Loop for Fine-Grained Power Management Unit. , 2018, , .		6
102	Adiabatically driven touch controller analog front-end for ultra-thin displays. , 2018, , .		6
103	A 4-to-20Gb/s 1.87pJ/b Referenceless Digital CDR With Unlimited Frequency Detection Capability in 65nm CMOS. , 2019, , .		6
104	A 15-GHz, 17.8-mW, 213-fs Injection-Locked PLL With Maximized Injection Strength Using Adjustment of Phase Domain Response. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1932-1936.	2.2	6
105	A single-inductor, multiple-channel current-balancing LED driver for display backlight applications. , 2013, , .		5
106	1.2 V 10-bit 75 MS/s Pipelined ADC With Phase-Dependent Gain-Transition CDS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 585-592.	2.1	5
107	A 7.6 mW, 214-fs RMS jitter 10-GHz phase-locked loop for 40-Gb/s serial link transmitter based on two-stage ring oscillator in 65-nm CMOS. , 2015, , .		5
108	Use of Phase Delay Analysis for Evaluating Wideband Circuits: An Alternative to Group Delay Analysis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3543-3547.	2.1	5

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109	A compact 87.1-dB DR bandwidth-scalable delta-sigma modulator based on dynamic gain-bandwidth-boosting inverter for audio applications. , 2017, , .		5
110	A Crystal-Less Programmable Clock Generator with RC-LC Hybrid Oscillator for GHz Applications in 14 nm FinFET CMOS. , 2018, , .		5
111	A 2.5â€“28 Gb/s Multi-Standard Transmitter With Two-Step Time-Multiplexing Driver. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1927-1931.	2.2	5
112	A 370-fJ/b, 0.0056 mm²/DQ, 4.8-Gb/s DQ Receiver for HBM3 with a Baud-Rate Self-Tracking Loop. , 2019, , .		5
113	A Maximum-Eye-Tracking CDR With Biased Data-Level and Eye Slope Detector for Near-Optimal Timing Adaptation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2708-2720.	2.1	5
114	32.4 A 0.4-to-1.2V 0.0057mm² 55fs-Transient-FoM Ring-Amplifier-Based Low-Dropout Regulator with Replica-Based PSR Enhancement. , 2020, , .		5
115	Design of Soft-Switching Hybrid DC-DC Converter with 2-Phase Switched Capacitor and 0.8nH Inductor for Standard CMOS Process. Electronics (Switzerland), 2020, 9, 372.	1.8	5
116	Analysis of frequency detection capability of Alexander phase detector. Electronics Letters, 2020, 56, 180-182.	0.5	5
117	A PVT Variation-Robust All-Digital Injection-Locked Clock Multiplier With Real-Time Offset Tracking Using Time-Division Dual Calibration. IEEE Journal of Solid-State Circuits, 2021, 56, 2525-2538.	3.5	5
118	A Residue-Current-Locked Hybrid Low-Dropout Regulator Supporting Ultralow Dropout of Sub-50 mV With Fast Settling Time Below 10 ns. IEEE Journal of Solid-State Circuits, 2022, 57, 2236-2249.	3.5	5
119	A 40-Gb/s transceiver in 0.13-μm CMOS technology. , 2008, , .		4
120	A PVT-insensitive time-to-digital converter using fractional difference Vernier delay lines. , 2009, , .		4
121	4-Slot, 8-Drop Impedance-Matched Bidirectional Multidrop DQ Bus With a 4.8-Gb/s Memory Controller Transceiver. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, 3, 858-869.	1.4	4
122	A 6.3 mW high-SNR frame-rate scalable touch screen panel readout IC with column-parallel Σ-Δ ADC structure for mobile devices. , 2013, , .		4
123	A Modulo-FIR Equalizer for Wireline Communications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4278-4286.	3.5	4
124	A 2.5â€“32 Gb/s Gen 5-PCIe Receiver With Multi-Rate CDR Engine and Hybrid DFE. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2677-2681.	2.2	4
125	A 48 Gb/s PAM4 receiver with Baud-rate phase-detector for multi-level signal modulation in 40 nm CMOS. , 2021, , .		4
126	A 64-Gb/s PAM-4 Receiver With Transition-Weighted Phase Detector. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3704-3708.	2.2	4

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127	A 62.5-250 MHz multi-phase delay-locked loop using a replica delay line with triply controlled delay cells. , 0, , .		3
128	An 8-bit 125 MS/s CMOS folding ADC for Gigabit Ethernet LSI. , 0, , .		3
129	A 5.6 GHz LC digitally controlled oscillator with high frequency resolution using novel quadruple resolution varactor. , 2010, , .		3
130	A 55.1 mW 1.62-to-8.1 Gb/s Video Interface Receiver Generating up to 680 MHz Stream Clock Over 20 dB Loss Channel. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1432-1436.	2.2	3
131	A 10-Gb/s, 0.03-mm², 1.28-pJ/bit Half-Rate Injection-Locked CDR With Path Mismatch Tracking Loop in a 28-nm CMOS Technology. IEEE Journal of Solid-State Circuits, 2019, 54, 2812-2822.	3.5	3
132	A Compact Self-Capacitance Sensing Analog Front-End for a Touch Detection in Low-Power Mode. , 2019, , .		3
133	A 48 Gb/s PAM-4 Transmitter With 3-Tap FFE Based on Double-Shielded Coplanar Waveguide in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1569-1573.	2.2	3
134	A 22-Gb/s 0.95-pJ/b Energy-Efficient Voltage-Mode Transmitter With Time-Based Feedforward Equalization in a 28-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1099-1106.	2.1	3
135	A Bandpass ΔΣ Interface IC for Sacrificial Bulk Micromachined Inertial Sensors. , 2006, , .		2
136	A 16-bit ultra-thin tri-axes capacitive microaccelerometer for mobile application. , 2007, , .		2
137	A 10-Gb/s optical receiver front-end with 5-mW transimpedance amplifier. , 2010, , .		2
138	A 10-Gb/s 6-V<inf>pp</inf> differential modulator driver in 65-nm CMOS. , 2014, , .		2
139	20-Gb/s 3.6-V<inf>PP</inf>-swing source-series-terminated driver with 2-Tap FFE in 65-nm CMOS. , 2015, , .		2
140	A 1.74mW/GHz 0.11â€“2.5GHz fast-locking, jitter-reducing, 180Â° phase-shift digital DLL with a window phase detector for LPDDR4 memory controllers. , 2015, , .		2
141	A low-power pulse position modulation transceiver. , 2015, , .		2
142	A 800-Mb/s 0.89-pJ/b reference-less optical receiver with pulse-position-modulation scheme. , 2016, , .		2
143	Realâ€time currentâ€sensing feedback system for compensating processâ€“voltageâ€“temperature variations of display using doubleâ€gate oxide TFT. Electronics Letters, 2017, 53, 117-119.	0.5	2
144	25-Gb/s Clocked Pluggable Optics for High-Density Data Center Interconnections. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1395-1399.	2.2	2

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145	An Always-On 0.53-to-13.4 mW Power-Scalable Touchscreen Controller for Ultrathin Touchscreen Displays With Current-Mode Filter and Incremental Hybrid Î”Î£ ADC. , 2019, , .		2
146	0.76-mW/pF/GHz, 7-GHz Quadrature Resonant Clock With Frequency Tuning Capacitor and Amplitude Control Feedback Loop. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 136-140.	2.2	2
147	A Clock Distribution Scheme Insensitive to Supply Voltage Drift With Self-Adjustment of Clock Buffer Delay. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 814-818.	2.2	2
148	A 1.93-pJ/Bit PCI Express Gen4 PHY Transmitter with On-Chip Supply Regulators in 28 nm CMOS. Electronics (Switzerland), 2021, 10, 68.	1.8	2
149	A 500 MHz-to-1.2 GHz Reset Free Delay Locked Loop for Memory Controller with Hysteresis Coarse Lock Detector. Journal of Semiconductor Technology and Science, 2011, 11, 73-79.	0.1	2
150	A 285-fs_{rms}Integrated Jitter Injection-Locked Ring PLL with Charge-Stored Complementary Switch Injection Technique. Journal of Semiconductor Technology and Science, 2016, 16, 860-866.	0.1	2
151	A 10 Gb/s PAM-4 Transmitter with Feed-Forward Implementation of Tomlinson-Harashima Precoding in 28 nm CMOS. IEEE Access, 2021, , 1-1.	2.6	2
152	A 1.05-to-3.2 GHz All-Digital PLL for DDR5 Registering Clock Driver With a Self-Biased Supply-Noise-Compensating Ring DCO. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 759-763.	2.2	2
153	Area and Power Efficient 10B6Q PAM-4 DC Balance Coder for Automotive Camera Link. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2056-2060.	2.2	2
154	A Low-Jitter 8-GHz RO-Based ADPLL With PVT-Robust Replica-Based Analog Closed Loop for Supply Noise Compensation. IEEE Journal of Solid-State Circuits, 2022, 57, 1712-1722.	3.5	2
155	A 48Gb/s 2.4pJ/b PAM-4 Baud-Rate Digital CDR with Stochastic Phase Detection Technique in 40nm CMOS. , 2021, , .		2
156	A 32-Gb/s PAM4-Binary Bridge With Sampler Offset Cancellation for Memory Testing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3749-3753.	2.2	2
157	A 32Ã—32 self-timed multiplier with early completion. , 0, , .		1
158	A 3-mW, 270-Mbps, Clock-Edge Modulated Serial Link for Mobile Displays. , 2005, , .		1
159	An 1.4Gbps/ch LVDS Receiver with Jitter-Boundary-Based Digital De-skew Algorithm. , 2006, , .		1
160	58.4: 10-Bit Column Driver with Split-DAC Architecture. Digest of Technical Papers SID International Symposium, 2008, 39, 892.	0.1	1
161	A 1.35GHz all-digital fractional-N PLL with adaptive loop gain controller and fractional divider. , 2009, , .		1
162	A 1.3–330-MHz direct clock synthesizer for display interface using fractional multimodulus frequency divider. , 2009, , .		1

#	Article	IF	Citations
163	A 5-Gb/s digitally controlled 3-tap DFE receiver for serial communications. , 2010, , .		1
164	250Mbps-5Gbps wide-range CDR with digital vernier phase shifting and dual mode control in 0.13. , 2010, , .		1
165	A 26.5 Gb/s optical receiver with all-digital clock and data recovery in 65nm CMOS process. , 2014, , .		1
166	Test of the VCSEL driver based on Verilog-A VCSEL model. , 2015, , .		1
167	A compact 22-Gb/s transmitter for optical links with all-digital phase-locked loop. , 2015, , .		1
168	25 Gb/s photoreceiver based on vertical-illumination type Ge-on-Si photodetector and CMOS amplifier circuit for optical interconnects. , 2015, , .		1
169	A 6-to-32 Gb/s voltage-mode transmitter with scalable supply, voltage swing, and pre-emphasis in 65-nm CMOS. , 2016, , .		1
170	A 10-Gb/s, 0.03-mm², 1.28-pJ/bit Half-Rate All-Digital Injection-Locked Clock and Data Recovery with Maximum Timing-Margin Tracking Loop. , 2018, , .		1
171	A 0.83-pJ/Bit 6.4-Gb/s HBM Base Die Receiver Using a 45Â° Strobe Phase for Energy-Efficient Skew Compensation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1735-1739.	2.2	1
172	A 0.45 pJ/b, 6.4 Gb/s Forwarded-Clock Receiver With DLL-Based Self-Tracking Loop for Unmatched Memory Interfaces. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1814-1818.	2.2	1
173	A Programmable On-Chip Reference Oscillator With Slow-Wave Coplanar Waveguide in 14-nm FinFET CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1834-1838.	2.2	1
174	Design of a Transceiver Transmitting Power, Clock, and Data over a Single Optical Fiber for Future Automotive Network System. Journal of Semiconductor Technology and Science, 2017, 17, 48-55.	0.1	1
175	A Combined Clock and Data Recovery Circuit with Adaptive Cancellation of Data-Dependent Jitter. Journal of Semiconductor Technology and Science, 2008, 8, 193-199.	0.1	1
176	A Sequential Two-step Algorithm For DC Offset Cancellation of PAM-4 Receiver. , 2021, , .		1
177	A 112-Gb/s PAM-4 Transmitter with 8:1 MUX in 28-nm CMOS. , 2020, , .		1
178	Design and implementation of OTCA MAC protocol for high-speed point-to-point ring network. , 0, , .		0
179	A 1.25-GBaud CMOS transceiver with on-chip terminator and voltage mode driver for Gigabit Ethernet 1000Base-X. , 0, , .		0
180	Full-CMOS 2.4 GHz wideband CDMA transmitter and receiver with direct conversion mixers and DC-offset cancellation. , 0, , .		0

#	Article	IF	Citations
181	A fully-integrated CMOS frequency synthesizer with charge-averaging charge pump and dual-path loop filter for PCS- and cellular-CDMA wireless systems. , 0, , .		0
182	Multi-channel capacitive readout IC for MEMS inertial sensors. , 2008, , .		0
183	Simultaneous control of power/ground current, wakeup time and transistor overhead in power gated circuits. , 2008, , .		0
184	27.3: 1.2 Gbps GDDR3 Physical Layer for 3D AMOLED Panel. Digest of Technical Papers SID International Symposium, 2011, 42, 357-360.	0.1	0
185	Design of CMOS 5 Gb/s 4-PAM transceiver frontend for low-power memory interface. , 2012, , .		0
186	12.5-Gb/s analog front-end of an optical transceiver in 0.13-μm CMOS. , 2013, , .		0
187	A study on using pulse generators to design a ring-VCO based bang-bang PLL/CDR with a consistent loop bandwidth. , 2014, , .		0
188	A theoretical analysis of phase shift in pulse injection-locked oscillators. , 2016, , .		0
189	100 Gb/s photoreceiver module based on 4ch Ã— 25 Gb/s vertical-illumination-type Ge-on-Si photodetectors and amplifier circuits. Proceedings of SPIE, 2016, , .	0.8	0
190	A PVT-compensated sinusoidal wave generator with phase modulation for multi-channel sensor applications. , 2018, , .		0
191	An injection-locked ADCDR with reference-less frequency tracking. , 2018, , .		0
192	A 16-Gb/s injection-locked CDR in embedded clock receiver. , 2018, , .		0
193	4-Channel Push-Pull VCSEL Drivers for HDMI Active Optical Cable in 0.18-Î¼m CMOS. , 2018, , .		0
194	A $4.7mu mathrm{A}$ Quiescent Current Synthesizable Digital Low Dropout Regulator in 28-nm CMOS. , 2019, , .		0
195	A Design of Data Path Based on CMOS Logic for a 72-Gb/s PAM-4 Transmitter in 28-nm CMOS. , 2019, , .		0
196	Balancing scheme for phase current and flyingâ€capacitor voltage in threeâ€level DCâ€“DC converter. Electronics Letters, 2020, 56, 426-428.	0.5	0
197	Synthesisable glitchâ€less phase rotator with conditionally cascading scheme. Electronics Letters, 2020, 56, 536-538.	0.5	0
198	An 8-GHz Octa-Phase Error Corrector With Coprime Phase Comparison Scheme in 40-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 874-878.	2.2	0

#	Article	IF	Citations
199	A Stochastic Variable Gain Amplifier Adaptation for PAM-4 signaling. , 2021, , .		0