Srikanth Parameswaran

List of Publications by Year
in descending order

130	1,445	840728 11	677123 22
papers	citations	h-index	g-index

137	137	137	1028
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Processor Design for Soft Errors. ACM Computing Surveys, 2017, 49, 1-44.	23.0	101
2	Minimally Biased Multipliers for Approximate Integer and Floating-Point Multiplication. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2623-2635.	2.7	60
3	darkNoC. , 2014, , .		53
4	GPU accelerated adaptive banded event alignment for rapid comparative nanopore signal analysis. BMC Bioinformatics, 2020, 21, 343.	2.6	53
5	Design methodology for pipelined heterogeneous multiprocessor system. Proceedings - Design Automation Conference, 2007, , .	0.0	48
6	IMPRES. , 2006, , .		43
7	Embedded systems securityâ€"an overview. Design Automation for Embedded Systems, 2008, 12, 173-183.	1.0	42
8	Dark silicon as a challenge for hardware/software co-design. , 2014, , .		42
9	Finding optimal L1 cache configuration for embedded systems. , 2006, , .		40
10	Fast nanopore sequencing data analysis with SLOW5. Nature Biotechnology, 2022, 40, 1026-1029.	17.5	40
11	Approximate Integer and Floating-Point Dividers with Near-Zero Error Bias. , 2019, , .		31
12	Hardware/software managed scratchpad memory for embedded system. , 0, , .		30
13	RIJID. Proceedings - Design Automation Conference, 2007, , .	0.0	29
14	MUTE-AES: A multiprocessor architecture to prevent power analysis based side channel attack of the AES algorithm. , 2008, , .		28
15	NoCOUT : NoC topology generation with mixed packet-switched and point-to-point networks. , 2008, , .		28
16	Heterogeneous multiprocessor implementations for JPEG:. , 2006, , .		26
17	A design flow for application specific heterogeneous pipelined multiprocessor systems. , 2009, , .		24
18	Rapid Design Space Exploration of Application Specific Heterogeneous Pipelined Multiprocessor Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1777-1789.	2.7	24

#	Article	IF	Citations
19	Optimal synthesis of latency and throughput constrained pipelined MPSoCs targeting streaming applications. , 2010, , .		23
20	Low-power adaptive pipelined MPSoCs for multimedia. , 2011, , .		22
21	Approximate Computing for ML. , 2021, , .		22
22	Advanced modes in AES: Are they safe from power analysis based side channel attacks?. , 2014, , .		21
23	SuSeSim. , 2009, , .		21
24	RASTER. , 2013, , .		20
25	SuperNet. , 2015, , .		19
26	EETD: An Energy Efficient Design for Runtime Hardware Trojan Detection in Untrusted Network-on-Chip. , 2018, , .		19
27	System-level application-aware dynamic power management in adaptive pipelined MPSoCs for multimedia. , 2011, , .		18
28	Partial Dynamic Element Matching Technique for Digital-to-Analog Converters Used for Digital Harmonic-Cancelling Sine-Wave Synthesis. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 296-309.	5.4	17
29	A smart random code injection to mask power analysis based side channel attacks. , 2007, , .		16
30	Architectural Frameworks for Security and Reliability of MPSoCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1641-1654.	3.1	14
31	Malleable NoC: Dark Silicon Inspired Adaptable Network-on-Chip. , 2015, , .		14
32	Featherweight long read alignment using partitioned reference indexes. Scientific Reports, 2019, 9, 4318.	3.3	14
33	Fidelity metrics for estimation models. , 2010, , .		13
34	A simple digital architecture for a harmonic-cancelling sine-wave synthesizer. , 2014, , .		13
35	RFTC. , 2019, , .		13
36	REALM: Reduced-Error Approximate Log-based Integer Multiplier. , 2020, , .		13

#	Article	IF	Citations
37	Synthesis of heterogeneous pipelined multiprocessor systems using ILP. , 2008, , .		13
38	Voltage reduction of application-specific heterogeneous multiprocessor systems for power minimisation. , 2000, , .		12
39	Energy-Efficient Adaptive Pipelined MPSoCs for Multimedia Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 663-676.	2.7	12
40	Novel architecture for loop acceleration. , 2005, , .		11
41	Performance Estimation of Pipelined MultiProcessor System-on-Chips (MPSoCs). IEEE Transactions on Parallel and Distributed Systems, 2014, 25, 2159-2168.	5.6	11
42	Architectural Exploration of Heterogeneous Multiprocessor Systems for JPEG. International Journal of Parallel Programming, 2008, 36, 140-162.	1.5	10
43	Side channel attacks in embedded systems: A tale of hostilities and deterrence. , 2015, , .		10
44	Overview and Investigation of SEU Detection and Recovery Approaches for FPGA-Based Heterogeneous Systems. , 2016, , 33-46.		10
45	TrojanGuard. , 2017, , .		10
46	LOP_RE: Range encoding for low power packet classification. , 2009, , .		9
47	Rapid runtime estimation methods for pipelined MPSoCs. , 2010, , .		9
48	A double-width algorithmic balancing to prevent power analysis Side Channel Attacks in AES. , 2013, , .		9
49	SCUD. , 2010, , .		8
50	Multi-ASIP based parallel and scalable implementation of motion estimation kernel for high definition videos. , 2011, , .		8
51	Design of a digital harmonic-cancelling sine-wave synthesizer with 100 MHz output frequency, 43.5 dB SFDR, and 2.26 mW power. , 2015, , .		8
52	Fine-Grained Checkpoint Recovery for Application-Specific Instruction-Set Processors. IEEE Transactions on Computers, 2017, 66, 647-660.	3.4	8
53	DEW: A fast level 1 cache simulation approach for embedded processors with FIFO replacement policy. , 2010, , .		7
54	Randomized Instruction Injection to Counter Power Analysis Attacks. Transactions on Embedded Computing Systems, 2012, 11, 1-28.	2.9	7

#	Article	IF	Citations
55	DHASER: Dynamic heterogeneous adaptation for soft-error resiliency in ASIP-based multi-core systems. , 2013, , .		7
56	A scorchingly fast FPGA-based Precise L1 LRU cache simulator. , 2014, , .		7
57	Dark Silicon. , 2015, , .		7
58	MESGA: An MPSoC based embedded system solution for short read genome alignment. , 2018, , .		7
59	Hardware Trojan Mitigation in Pipelined MPSoCs. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-27.	2.6	7
60	INSIDE: INstruction Selection/Identification & Design Exploration for extensible processors. , 2003, , .		6
61	Energy Driven Application SelfAdaptation. , 2007, , .		6
62	HitME: Low power Hit MEmory buffer for embedded systems. , 2009, , .		6
63	LOP. , 2009, , .		6
64	Run-time adaption for highly-complex multi-core systems. , 2013, , .		6
65	NORA: Algorithmic Balancing without Pre-charge to Thwart Power Analysis Attacks. , 2017, , .		6
66	DoSGuard: Protecting pipelined MPSoCs against hardware Trojan based DoS attacks. , 2017, , .		6
67	CryptoBlaze: A partially homomorphic processor with multiple instructions and non-deterministic encryption support. , 2018, , .		6
68	DIMSim. , 2012, , .		5
69	A Rapid Methodology for Multi-mode Communication Circuit Generation. , 2012, , .		5
70	MAPro: A Tiny Processor for Reconfigurable Baseband Modulation Mapping. , 2013, , .		5
71	CSER: HW/SW Configurable Soft-Error Resiliency for Application Specific Instruction-Set Processors. , 2013, , .		5
72	RExCache: Rapid exploration of unified last-level cache. , 2013, , .		5

#	Article	IF	Citations
73	QuadSeal: Quadruple algorithmic symmetrizing countermeasure against power based side-channel attacks. , 2015, , .		5
74	UCloD: Small Clock Delays to Mitigate Remote Power Analysis Attacks. IEEE Access, 2021, 9, 108411-108425.	4.2	5
75	Profiling in the ASP codesign environment. Journal of Systems Architecture, 2000, 46, 1263-1274.	4.3	4
76	A digital ultra-wideband multiband transceiver architecture with fast frequency hopping capabilities. , 0, , .		4
77	Instruction Trace Compression for Rapid Instruction Cache Simulation. , 2007, , .		4
78	CIPARSim: Cache intersection property assisted rapid single-pass FIFO cache simulation technique. , 2011, , .		4
79	Realizing Cycle Accurate Processor Memory Simulation via Interface Abstraction. , 2011, , .		4
80	A Hardware/Software Countermeasure and a Testing Framework for Cache Based Side Channel Attacks. , 2011, , .		4
81	XDRA. , 2013, , .		4
82	MASH{fifo}. , 2014, , .		4
83	Pairwise alignment of nucleotide sequences using maximal exact matches. BMC Bioinformatics, 2019, 20, 261.	2.6	4
84	RECORD: Reducing Register Traffic for Checkpointing in Embedded Processors. , 2016, , .		4
85	Anatomy of Differential Power Analysis for AES. , 2008, , .		3
86	MCAD: Multiple connection based anomaly detection. , 2008, , .		3
87	Fine-grained hardware/software methodology for process migration in MPSoCs. , 2012, , .		3
88	Reli: Hardware/software Checkpoint and Recovery scheme for embedded processors. , 2012, , .		3
89	Dynamic encryption key design and management for memory data encryption in embedded systems. , 2013, , .		3
90	Reconfigurable Convolutional Codec for Physical Layer Communication Security Application. , 2014, , .		3

#	Article	IF	Citations
91	SDG2KPN: System Dependency Graph to function-level KPN generation of legacy code for MPSoCs. , 2014, , .		3
92	Dynamic Reconfigurable Puncturing for Secure Wireless Communication. , 2015, , .		3
93	ARGUS: A Framework for Rapid Design and Prototype of Heterogeneous Multicore Systems in FPGA. , 2015, , .		3
94	FINDER: Find Efficient Parallel Instructions for ASIPs to Improve Performance of Large Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3577-3588.	2.7	3
95	LOCS. , 2008, , .		3
96	Multi-mode pipelined MPSoCs for streaming applications. , 2013, , .		2
97	Latency-constrained binding of data flow graphs to energy conscious GALS-based MPSoCs. , 2013, , .		2
98	Hardware-based fast exploration of cache hierarchies in application specific MPSoCs. , 2014, , .		2
99	E-pipeline: Elastic Hardware/Software Pipelines on a Many-Core Fabric. , 2015, , .		2
100	Exploring Multilevel Cache Hierarchies in Application Specific MPSoCs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1991-2003.	2.7	2
101	ADAPT: An adaptive manycore methodology for software pipelined applications. , 2015, , .		2
102	Network-on-Chip Design. , 2017, , 461-489.		2
103	Balancing System Level Pipelines with Stage Voltage Scaling. , 0, , .		1
104	Automatic Application Specific Floating-point Unit Generation. , 2007, , .		1
105	CoRaS: A multiprocessor key corruption and random round swapping for power analysis side channel attacks: A DES case study. , 2012, , .		1
106	Energy-aware synthesis of application specific MPSoCs. , 2013, , .		1
107	A survey on exact cache design space exploration methodologies for application specific SoC memory hierarchies. , 2013, , .		1
108	Hardware-based fast exploration of cache hierarchies in application specific MPSoCs. , 2014, , .		1

#	Article	IF	Citations
109	RAPITIMATE: Rapid performance estimation of pipelined processing systems containing shared memory. , 2015, , .		1
110	Sequential C-code to distributed pipelined heterogeneous MPSoC synthesis for streaming applications. , 2015, , .		1
111	The effect of amplitude resolution and mismatch on a digital-to-analog converter used for digital harmonic-cancelling sine-wave synthesis. , 2016, , .		1
112	Switchable cache: utilising dark silicon for application specific cache optimisations. IET Computers and Digital Techniques, 2016, 10, 157-164.	1.2	1
113	Adroit Use of Dark Silicon for Power, Performance and Reliability Optimisation of NoCs. , 2017, , 291-325.		1
114	Guest editorial for special issue on embedded systemÂsecurity. Design Automation for Embedded Systems, 2008, 12, 171-172.	1.0	0
115	CUFFS: An instruction count based architectural framework for security of MPSoCs. , 2009, , .		0
116	Improved Architectures for Range Encoding in Packet Classification System. , 2010, , .		0
117	A Study on Instruction-set Selection Using Multi-application Based Application Specific Instruction-set Processors. , 2013, , .		0
118	Variable increment step based reconfigurable interleaver for multimode communication application. , 2013, , .		0
119	A case study on exploration of last-level cache for energy reduction in DDR3 DRAM. , 2013, , .		0
120	An Extremely Compact JPEG Encoder for Adaptive Embedded Systems. , 2013, , .		0
121	System-level optimization of on-chip communication using express links for throughput constrained MPSoCs. , 2013, , .		0
122	Mapping programs for execution on pipelined MPSoCs. , 2014, , .		0
123	Flexible and scalable implementation of H.264/AVC encoder for multiple resolutions using ASIPs. , 2014, , .		0
124	Flexible and scalable implementation of H.264/AVC encoder for multiple resolutions using ASIPs. , 2014, , .		0
125	Speeding up single pass simulation of PLRUt caches. , 2015, , .		0
126	ARCHER: Communication-based predictive architecture selection for application specific multiprocessor Systems-on-Chip. , 2015, , .		0

#	Article	IF	Citations
127	Hardware Trojan Detection and Recovery in MPSoCs via On-line Application Specific Testing. , 2019, , .		0
128	Optimisation Framework. , 2014, , 53-64.		0
129	Network-on-Chip Design. , 2016, , 1-29.		0
130	SHORE: Hardware/Software Method for Memory Safety Acceleration on RISC-V. , 2021, , .		0