Daniel Munari Palomino

List of Publications by Year
in descending order

62	281	1937685 4	1720034 7
papers	citations	h-index	g-index

62	62	62	141
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	FastInter360: A Fast Inter Mode Decision for HEVC 360 Video Coding. IEEE Transactions on Circuits and Systems for Video Technology, 2022, 32, 3235-3249.	8.3	7
2	Power-Quality Configurable Hardware Design for AV1 Directional Intraframe Prediction. IEEE Design and Test, 2022, 39, 38-45.	1.2	2
3	Low-Complexity HEVC Transrating Based on Prediction Unit Mode Inheritance. , 2021, , .		1
4	AV1 and VVC Video Codecs: Overview on Complexity Reduction and Hardware Design. IEEE Open Journal of Circuits and Systems, 2021, 2, 564-576.	1.9	2
5	Exploring Operation Sharing in Directional Intra Frame Prediction of AV1 Video Coding. , 2021, , .		0
6	Modern Video Coding: Methods, Challenges and Systems. Journal of Integrated Circuits and Systems, 2021, 16, 1-12.	0.4	1
7	ESA360 - Early SKIP Mode Decision Algorithm for Fast ERP 360 Video Coding. , 2021, , .		2
8	Fast Block Size Decision for HEVC Encoders with On-the-Fly Trained Classifiers. , 2021, , .		2
9	Fast VP9-to-AV1 Transcoding based on Block Partitioning Inheritance. , 2021, , .		3
10	Speedup evaluation of HEVC parallel video coding using Tiles. Journal of Real-Time Image Processing, 2020, 17, 1469-1486.	3.5	2
11	Efficient Hardware Design for the AV1 CDEF Filter Targeting 4K UHD Videos. , 2020, , .		4
12	Low-Power and Memory-Aware Approximate Hardware Architecture for Fractional Motion Estimation Interpolation on HEVC. , 2020, , .		5
13	ASIC Solution for the Directional Intra Prediction of the AV1 Encoder Targeting UHD 4K Videos. , 2020, , .		8
14	Directional Intra Frame Prediction Architecture with Edge Filter and Upsampling for AV1 Video Coding. , 2020, , .		6
15	Spatially Adaptive Intra Mode Pre-Selection for ERP 360 Video Coding. , 2020, , .		5
16	RDE-MOGA: Automatic Selection of Rate-Distortion-Energy Control Points for Video Encoders Using Muti-Objetive Genetic Algorithm. , 2020, , .		0
17	6WR: A Hardware Friendly 3D-HEVC DMM-1 Algorithm and its Energy-Aware and High-Throughput Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 836-840.	3.0	1
18	A High-Throughput Hardware Architecture for AV1 Non-Directional Intra Modes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1481-1494.	5.4	10

#	Article	IF	Citations
19	Real-Time and Low-Power HEVC Deblocking Filter Architecture Targeting 8K UHD @ 60fps Videos. Journal of Integrated Circuits and Systems, 2020, 15, 1-9.	0.4	3
20	Memory-aware Workload Balancing Technique based on Decision Trees for Parallel HEVC Video Coding. Journal of Integrated Circuits and Systems, 2020, 15, 1-9.	0.4	0
21	ERP-Based CTU Splitting Early Termination for Intra Prediction of 360 videos. , 2020, , .		3
22	Power/QoS-Adaptive HEVC FME Hardware using Machine Learning-Based Approximation Control. , 2020, , .		0
23	4D-DCT Hardware Architecture for JPEG Pleno Light Field Coding. , 2020, , .		1
24	An Overview of Dedicated Hardware Designs for State-of-the-Art AV1 and H.266/VVC Video Codecs. , 2020, , .		8
25	High Throughput Hardware Design for AV1 Paeth and Smooth Intra Modes. , 2019, , .		11
26	Online Machine Learning for Fast Coding Unit Decisions in HEVC. , 2019, , .		2
27	Encoding Efficiency and Computational Cost Assessment of State-Of-The-Art Point Cloud Codecs. , 2019, , .		3
28	High-Throughput Multifilter Interpolation Architecture for AV1 Motion Compensation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 883-887.	3.0	19
29	A High Throughput Hardware Architecture Targeting the AV1 Paeth Intra Predictor. , 2019, , .		10
30	Low-Power and High-Throughput Approximate 4Ã—4 DCT Hardware Architecture. , 2019, , .		1
31	Energy-Efficiency Exploration of Memory Hierarchy using NVMs for HEVC Motion Estimation. , 2019, , .		4
32	Design Space Exploration of HEVC RCL Mapped onto NoC-Based Embedded Platforms. , 2019, , .		1
33	A New Hardware Friendly 2D-DCT HEVC Compliant Algorithm and its High Throughput and Low Power Hardware Design. , 2019, , .		3
34	Compression Efficiency and Computational Cost Comparison between AV1 and HEVC Encoders. , 2019, , .		4
35	Performance evaluation of HEVC RCL applications mapped onto NoC-based embedded platforms. , 2019, , .		0
36	A Fast Local Mode Decision for the HEVC Intra Prediction Based on Direction Detection. , 2019, , .		2

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37	Power-Efficient and Memory-Aware Approximate Hardware Design for HEVC FME Interpolator. , 2018, , .		4
38	Memory-Aware Tiles Workload Balance through Machine-Learnt Complexity Reduction for HEVC. , 2018, , .		3
39	Low-Power HEVC 1-D IDCT Hardware Architecture. , 2018, , .		1
40	High-Throughput and Low-Power Integrated Direct/Inverse HEVC Quantization Hardware Design. , 2018, , .		1
41	Configurable Cache Memory Architecture for Low-Energy Motion Estimation. , 2018, , .		6
42	OTED: Encoding Optimization Technique Targeting Energy-Efficient HEVC Decoding. , 2018, , .		5
43	Speedup-Oriented History-Based Tiling Algorithm for the HEVC Standard Targeting an Efficient Parallelism Exploration. Journal of Integrated Circuits and Systems, 2018, 13, 1-8.	0.4	1
44	Energy evaluation of the HEVC decoding for different encoding configurations. , 2017, , .		1
45	Cache Memory Energy Efficiency Exploration for the HEVC Motion Estimation. , 2017, , .		2
46	Speedup-aware history-based tiling algorithm for the HEVC standard. , 2016, , .		11
47	Adjusting video tiling to available resources in a per-frame basis in High Efficiency Video Coding. , 2016, , .		3
48	hevcDTM: Application-driven Dynamic Thermal Management for High Efficiency Video Coding. , 2014, , .		4
49	TONE. , 2014, , .		8
50	Adaptive content-based Tile partitioning algorithm for the HEVC standard. , 2013, , .		21
51	Fast HEVC intra mode decision algorithm based on new evaluation order in the Coding Tree Block. , 2013, , .		9
52	A memory aware and multiplierless VLSI architecture for the complete Intra Prediction of the HEVC emerging standard. , 2012, , .		31
53	Low-Complexity Hierarchical Mode Decision Algorithms Targeting VLSI Architecture Design for the H.264/AVC Video Encoder. VLSI Design, 2012, 2012, 1-20.	0.5	4
54	Algorithm and Hardware Design of a Fast Intra Frame Mode Decision Module for H.264/AVC Encoders. International Journal of Reconfigurable Computing, 2012, 2012, 1-10.	0.2	2

#	Article	IF	Citations
55	Algorithm and hardware design of a fast intra-frame mode decision module for h.264/AVC encoders. , 2011, , .		4
56	A high throughput H.264/AVC intra-frame encoding loop architecture for HD1080p. , 2011, , .		11
57	SHBS: A heuristic for fast inter mode decision of H.264/AVC standard targeting VLSI design. , 2011, , .		2
58	Homogeneity and distortion-based intra mode decision architecture for H.264/AVC. , 2010, , .		6
59	Low latency and high throughput dedicated loop of transforms and quantization focusing in the H.264/AVC Intra Prediction. , 2009, , .		0
60	Transforms and quantization design targeting the H.264/AVC intra prediction constraints. , 2009, , .		4
61	A multitransform architecture for the H.264/AVC standard and its design space exploration. , 2009, , .		1
62	Energy-Efficient NoC-Based Systems for Real-Time Multimedia Applications using Approximate Computing. , 0, , .		0