Mengwei Si

List of Publications by Year
in descending order

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		196777	139680
95	4,036	29	61
papers	citations	h-index	g-index

95	95	95	5480
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	First demonstration of robust tri-gate Î²-Ga₂O₃ nano-membrane field-effect transistors. Nanotechnology, 2022, 33, 125201.	1.3	11
2	Positive Bias Temperature Instability and Hot Carrier Degradation of Back-End-of-Line, nm-Thick, In₂O₃ Thin-Film Transistors. IEEE Electron Device Letters, 2022, 43, 232-235.	2.2	10
3	Controlling Threshold Voltage of CMOS SOI Nanowire FETs With Sub-1 nm Dipole Layers Formed by Atomic Layer Deposition. IEEE Transactions on Electron Devices, 2022, 69, 851-856.	1.6	5
4	Ionic Control over Ferroelectricity in 2D Layered van der Waals Capacitors. ACS Applied Materials & Interfaces, 2022, 14, 3018-3026.	4.0	16
5	Realization of Maximum 2 A/mm Drain Current on Top-Gate Atomic-Layer-Thin Indium Oxide Transistors by Thermal Engineering. IEEE Transactions on Electron Devices, 2022, 69, 147-151.	1.6	14
6	Enhancement of Thermal Transfer From Î²-Ga₂O₃ Nano-Membrane Field-Effect Transistors to High Thermal Conductivity Substrate by Inserting an Interlayer. IEEE Transactions on Electron Devices, 2022, 69, 1186-1190.	1.6	7
7	Atomically Thin Indium-Tin-Oxide Transistors Enabled by Atomic Layer Deposition. IEEE Transactions on Electron Devices, 2022, 69, 231-236.	1.6	20
8	Scaled indium oxide transistors fabricated using atomic layer deposition. Nature Electronics, 2022, 5, 164-170.	13.1	98
9	BEOL-Compatible, ALD-grown In₂O₃ Top-Gate FETs with Maximum Drain Current of 3 A/mm through Thermal Engineering and Pulse Measurement. , 2022, , .		2
10	Characterization of Interface and Bulk Traps in Ultrathin Atomic Layer-Deposited Oxide Semiconductor MOS Capacitors With HfO2/In2O3 Gate Stack by C-V and Conductance Method. Frontiers in Materials, 2022, 9, .	1.2	4
11	Vertically stacked multilayer atomic-layer-deposited sub-1-nm In2O3 field-effect transistors with back-end-of-line compatibility. Applied Physics Letters, 2022, 120, .	1.5	7
12	20â€3: Invited Paper: BEOLâ€Compatible Ferroelectric Fieldâ€Effect Transistors with Atomic Layer Deposition of Oxide Semiconductor Channel Toward Monolithic 3D Integration. Digest of Technical Papers SID International Symposium, 2022, 53, 221-224.	0.1	0
13	High-Performance Atomic-Layer-Deposited Indium Oxide 3-D Transistors and Integrated Circuits for Monolithic 3-D Integration. IEEE Transactions on Electron Devices, 2021, 68, 6605-6609.	1.6	19
14	Enhancement-mode atomic-layer thin In2O3 transistors with maximum current exceeding 2 A/mm at drain voltage of 0.7 V enabled by oxygen plasma treatment. Applied Physics Letters, 2021, 118, .	1.5	27
15	Scaled Atomic-Layer-Deposited Indium Oxide Nanometer Transistors With Maximum Drain Current Exceeding 2 A/mm at Drain Voltage of 0.7 V. IEEE Electron Device Letters, 2021, 42, 184-187.	2.2	48
16	Asymmetric Metal/Î±-In₂Se₃/Si Crossbar Ferroelectric Semiconductor Junction. ACS Nano, 2021, 15, 5689-5695.	7.3	36
17	Enhancement-Mode Atomic-Layer-Deposited In₂O₃ Transistors With Maximum Drain Current of 2.2 A/mm at Drain Voltage of 0.7 V by Low-Temperature Annealing and Stability in Hydrogen Environment. IEEE Transactions on Electron Devices, 2021, 68, 1075-1080.	1.6	36
18	Quantitative Characterization of Ferroelectric/Dielectric Interface Traps by Pulse Measurements. IEEE Transactions on Electron Devices, 2021, 68, 1214-1220.	1.6	14

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19	BEOL Compatible Indium-Tin-Oxide Transistors: Switching of Ultra-High-Density 2D Electron Gas over 0.8Ã—1014 /cm2 by Ferroelectric Polarization. , 2021, , .		0
20	First Experimental Demonstration of Robust HZO/Î²-Gaâ„Oâ‚ƒ Ferroelectric Field-Effect Transistors as Synaptic Devices for Artificial Intelligence Applications in a High-Temperature Environment. IEEE Transactions on Electron Devices, 2021, 68, 2515-2521.	1.6	14
21	Ultrathin transparent Copper(I) oxide films grown by plasma-enhanced atomic layer deposition for Back-end-of-line p-Type transistors. Nano Express, 2021, 2, 020023.	1.2	3
22	BEOL Compatible Indium-Tin-Oxide Transistors: Switching of Ultrahigh-Density 2-D Electron Gas Over 0.8 Ã— 10¹⁴/cm² at Oxide/Oxide Interface by the Change of Ferroelectric Polarization. IEEE Transactions on Electron Devices, 2021, 68, 3195-3199.	1.6	20
23	High-Performance Inâ„Oâ‚ƒ-Based 1T1R FET for BEOL Memory Application. IEEE Transactions on Electron Devices, 2021, 68, 3775-3779.	1.6	3
24	Polarization switching in Hf0.5Zr0.5O2-dielectric stack: The role of dielectric layer thickness. Applied Physics Letters, 2021, 119, .	1.5	8
25	Bilayer Quantum Hall States in an n-Type Wide Tellurium Quantum Well. Nano Letters, 2021, 21, 7527-7533.	4.5	6
26	The Critical Role of Charge Balance on the Memory Characteristics of Ferroelectric Field-Effect Transistors. IEEE Transactions on Electron Devices, 2021, 68, 5108-5113.	1.6	10
27	Why In₂O₃ Can Make 0.7 nm Atomic Layer Thin Transistors. Nano Letters, 2021, 21, 500-506.	4.5	99
28	Ferroelectric FET Based Coupled-Oscillatory Network for Edge Detection. IEEE Electron Device Letters, 2021, 42, 1670-1673.	2.2	5
29	Overview and outlook of emerging non-volatile memories. MRS Bulletin, 2021, 46, 946-958.	1.7	22
30	Indiumâ€“Tin-Oxide Transistors with One Nanometer Thick Channel and Ferroelectric Gating. ACS Nano, 2020, 14, 11542-11547.	7.3	75
31	The Impact of Channel Semiconductor on the Memory Characteristics of Ferroelectric Field-Effect Transistors. IEEE Journal of the Electron Devices Society, 2020, 8, 846-849.	1.2	8
32	Quantitative Characterization of Interface Traps in Ferroelectric/Dielectric Stack Using Conductance Method. IEEE Transactions on Electron Devices, 2020, 67, 5315-5321.	1.6	23
33	Î± -In2Se3 based ferroelectric-semiconductor metal junction for non-volatile memories. Applied Physics Letters, 2020, 117, .	1.5	22
34	Gate-tunable strong spin-orbit interaction in two-dimensional tellurium probed by weak antilocalization. Physical Review B, 2020, 101, .	1.1	29
35	Alignment of Polarization against an Electric Field in van der Waals Ferroelectrics. Physical Review Applied, 2020, 13, .	1.5	34
36	Quantum Hall effect of Weyl fermions in n-type semiconducting tellurene. Nature Nanotechnology, 2020, 15, 585-591.	15.6	63

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37	Record Fast Polarization Switching Observed in Ferroelectric Hafnium Oxide Crossbar Arrays. , 2020, , .		8
38	Raman response and transport properties of tellurium atomic chains encapsulated in nanotubes. Nature Electronics, 2020, 3, 141-147.	13.1	126
39	Single Pulse Charge Pumping Measurements on GaN MOS-HEMTs: Fast and Reliable Extraction of Interface Traps Density. IEEE Transactions on Electron Devices, 2020, 67, 444-448.	1.6	11
40	A tunable ferroelectric based unreleased RF resonator. Microsystems and Nanoengineering, 2020, 6, 8.	3.4	21
41	Field-Effect Transistors 4. Springer Series in Materials Science, 2020, , 623-638.	0.4	1
42	Low-Frequency Noise in IIIâ€“V, Ge, and 2D Transistors. , 2020, , 335-357.		0
43	Ultrafast measurements of polarization switching dynamics on ferroelectric and anti-ferroelectric hafnium zirconium oxide. Applied Physics Letters, 2019, 115, .	1.5	77
44	Room-Temperature Electrocaloric Effect in Layered Ferroelectric CuInP₂S₆ for Solid-State Refrigeration. ACS Nano, 2019, 13, 8760-8765.	7.3	69
45	Experimental Extraction of Ballisticity in Germanium Nanowire nMOSFETs. IEEE Transactions on Electron Devices, 2019, 66, 3541-3548.	1.6	4
46	Switchable Mechanical Resonance Induced by Hysteretic Piezoelectricity in Ferroelectric Capacitors. , 2019, , .		8
47	High Performance ${eta}$ -Ga₂O₃ Nano-Membrane Field Effect Transistors on a High Thermal Conductivity Diamond Substrate. IEEE Journal of the Electron Devices Society, 2019, 7, 914-918.	1.2	42
48	Ferroelectric Polarization Switching of Hafnium Zirconium Oxide in a Ferroelectric/Dielectric Stack. ACS Applied Electronic Materials, 2019, 1, 745-751.	2.0	66
49	A critical review of recent progress on negative capacitance field-effect transistors. Applied Physics Letters, 2019, 114, .	1.5	157
50	Modeling of Leakage-Assist-Switching in Ferroelectric/Dielectric Stack. , 2019, , .		0
51	Solar-Blind UV Photodetector Based on Atomic Layer-Deposited Cu₂O and Nanomembrane Î²-Ga₂O₃ pn Oxide Heterojunction. ACS Omega, 2019, 4, 20756-20761.	1.6	35
52	A ferroelectric semiconductor field-effect transistor. Nature Electronics, 2019, 2, 580-586.	13.1	317
53	Hybrid dual-channel phototransistor based on 1D t-Se and 2D ReS2 mixed-dimensional heterostructures. Nano Research, 2019, 12, 669-674.	5.8	34
54	(Invited) Raman Thermography of Î²-Ga2ÂO3 Nanomembrane FETs on Diamond. ECS Meeting Abstracts, 2019, , .	0.0	0

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55	(Invited) A Ferroelectric Semiconductor Field-Effect Transistor. ECS Meeting Abstracts, 2019, , .	0.0	0
56	A Closed Form Analytical Model of Back-Gated 2-D Semiconductor Negative Capacitance Field Effect Transistors. IEEE Journal of the Electron Devices Society, 2018, 6, 189-194.	1.2	35
57	Carrier Mobility Enhancement by Applying Back-Gate Bias in Ge-on-Insulator MOSFETs. IEEE Electron Device Letters, 2018, 39, 176-179.	2.2	9
58	Mobility Fluctuation-Induced Low-Frequency Noise in Ultrascaled Ge Nanowire nMOSFETs With Near-Ballistic Transport. IEEE Transactions on Electron Devices, 2018, 65, 2573-2577.	1.6	5
59	Thermoreflectance imaging of electromigration evolution in asymmetric aluminum constrictions. Journal of Applied Physics, 2018, 123, 035107.	1.1	2
60	Steep-slope hysteresis-free negative capacitance MoS2 transistors. Nature Nanotechnology, 2018, 13, 24-28.	15.6	422
61	High-Performance Few-Layer Tellurium CMOS Devices Enabled by Atomic Layer Deposited Dielectric Doping Technique. , 2018, , .		16
62	First Demonstration of Ge Ferroelectric Nanowire FET as Synaptic Device for Online Learning in Neural Network with High Number of Conductance State and G<inf>max</inf>/G<inf>min</inf>. , 2018, , .		28
63	First Direct Experimental Studies of Hf<inf>0.5</inf>Zr<inf>0.5</inf>O<inf>2</inf> Ferroelectric Polarization Switching Down to 100-picosecond in Sub-60mV/dec Germanium Ferroelectric Nanowire FETs. , 2018, , .		7
64	Time Response of Polarization Switching in Ge Hafnium Zirconium Oxide Nanowire Ferroelectric Field-effect Transistors. , 2018, , .		1
65	Ultraviolet Light-Based Currentâ€“Voltage Method for Simultaneous Extraction of Donor- and Acceptor-Like Interface Traps in <inline-formula> <tex-math notation="LaTeX">eta </tex-math> </inline-formula>-Ga₂O₃ FETs. IEEE Electron Device Letters, 2018, 39, 1708-1711.	2.2	14
66	Low frequency noise in MOS<inf>2</inf> negative capacitance field-effect transistor. , 2018, , .		0
67	Ferroelectric Field-Effect Transistors Based on MoS₂ and CuInP₂S₆ Two-Dimensional van der Waals Heterostructure. ACS Nano, 2018, 12, 6700-6705.	7.3	246
68	Steep slope 2D negative capacitance CMOS devices: MoS<inf>2</inf> and WSe<inf>2</inf>. , 2018, , .		0
69	Steep-Slope WSe₂ Negative Capacitance Field-Effect Transistor. Nano Letters, 2018, 18, 3682-3687.	4.5	97
70	2D Ferroelectric $pmb{mathrm{CuInP}_{2}mathrm{S}_{6}}$: Synthesis, ReRAM, and FeRAM. , 2018, , .		0
71	Alleviation of Short Channel Effects in Ge Negative Capacitance pFinFETs. , 2018, , .		4
72	Fin-Width Effects on Characteristics of InGaAs-Based Independent Double-Gate FinFETs. IEEE Electron Device Letters, 2017, 38, 441-444.	2.2	11

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73	One-Dimensional van der Waals Material Tellurium: Raman Spectroscopy under Strain and Magneto-Transport. Nano Letters, 2017, 17, 3965-3973.	4.5	272
74	High-Performance Depletion/Enhancement-ode eta -Ga2O3 on Insulator (GOOI) Field-Effect Transistors With Record Drain Currents of 600/450 mA/mm. IEEE Electron Device Letters, 2017, 38, 103-106.	2.2	247
75	Î²-Ga₂O₃ Nanomembrane Negative Capacitance Field-Effect Transistors with Steep Subthreshold Slope for Wide Band Gap Logic Applications. ACS Omega, 2017, 2, 7136-7140.	1.6	41
76	Anomalous bias temperature instability on accumulation-mode Ge and III-V MOSFETs. , 2017, , .		0
77	Black phosphorus field-effect transistor with record drain current exceeding 1 A/mm. , 2017, , .		12
78	Non-diffusive heat transport in twin nanoheater lines on silicon. , 2017, , .		0
79	Hysteresis-free negative capacitance germanium CMOS FinFETs with Bi-directional Sub-60 mV/dec. , 2017, , .		44
80	Al2O3/ $eta $ -Ga2O3(-201) Interface Improvement Through Piranha Pretreatment and Postdeposition Annealing. IEEE Electron Device Letters, 2016, 37, 1411-1414.	2.2	109
81	Demonstration of Ge Nanowire CMOS Devices and Circuits for Ultimate Scaling. IEEE Transactions on Electron Devices, 2016, , 1-9.	1.6	15
82	RTN and low frequency noise on ultra-scaled near-ballistic Ge nanowire nMOSFETs. , 2016, , .		1
83	High-Performance InAlN/GaN MOSHEMTs Enabled by Atomic Layer Epitaxy MgCaO as Gate Dielectric. IEEE Electron Device Letters, 2016, 37, 556-559.	2.2	46
84	Low-Frequency Noise and Random Telegraph Noise on Near-Ballistic III-V MOSFETs. IEEE Transactions on Electron Devices, 2015, 62, 3508-3515.	1.6	40
85	Demonstration of Ge CMOS inverter and ring oscillator with 10 nm ultra-thin channel. , 2015, , .		4
86	Germanium nMOSFETs With Recessed Channel and S/D: Contact, Scalability, Interface, and Drain Current Exceeding 1 A/mm. IEEE Transactions on Electron Devices, 2015, 62, 1419-1426.	1.6	27
87	First experimental demonstration of Ge 3D FinFET CMOS circuits. , 2015, , .		26
88	Inversion-mode GaAs wave-shaped field-effect transistor on GaAs (100) substrate. Applied Physics Letters, 2015, 106, 073506.	1.5	4
89	Ge CMOS: Breakthroughs of nFETs (I<inf>max</inf>=714 mA/mm,) Tj ETQq1 1 0.784314 rgBT /Overlock 10 Tf 50 102 Td (g&		10
90	Deep sub-100 nm Ge CMOS devices on Si with the recessed S/D and channel. , 2014, , .		13

#	Article	IF	Citations
91	The Effect of Dielectric Capping on Few-Layer Phosphorene Transistors: Tuning the Schottky Barrier Heights. IEEE Electron Device Letters, 2014, 35, 795-797.	2.2	154
92	Performance and Variability Studies of InGaAs Gate-all-Around Nanowire MOSFETs. IEEE Transactions on Device and Materials Reliability, 2013, 13, 489-496.	1.5	15
93	Molecular Doping of Multilayer ${m MoS}_{2}$ Field-Effect Transistors: Reduction in Sheet and Contact Resistances. IEEE Electron Device Letters, 2013, 34, 1328-1330.	2.2	231
94	Simple Noise Margin Model for Optimal Design of Unipolar Thin-Film Transistor Logic Circuits. IEEE Transactions on Electron Devices, 2013, 60, 1782-1785.	1.6	11
95	Effects of forming gas anneal on ultrathin InGaAs nanowire metal-oxide-semiconductor field-effect transistors. Applied Physics Letters, 2013, 102, 093505.	1.5	23