

Song Chen

List of Publications by Year in descending order

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109
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109
times ranked

294
citing authors

#	ARTICLE	IF	CITATIONS
1	Fixed-Outline Floorplanning: Block-Position Enumeration and a New Method for Calculating Area Costs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 858-871.	1.9	60
2	A Resource-Efficient Pipelined Architecture for Real-Time Semi-Global Stereo Matching. IEEE Transactions on Circuits and Systems for Video Technology, 2022, 32, 660-673.	5.6	24
3	Multi-layer floorplanning for stacked ICs: Configuration number and fixed-outline constraints. The Integration VLSI Journal, 2010, 43, 378-388.	1.3	22
4	Clustered Fault Tolerance TSV Planning for 3-D Integrated Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1287-1300.	1.9	22
5	Delay-driven layer assignment in global routing under multi-tier interconnect structure. , 2013, , .		20
6	Fast thermal analysis for fixed-outline 3D floorplanning. The Integration VLSI Journal, 2017, 59, 157-167.	1.3	20
7	Combining the ant system algorithm and simulated annealing for 3D/2D fixed-outline floorplanning. Applied Soft Computing Journal, 2016, 40, 150-160.	4.1	18
8	Application-specific Network-on-Chip synthesis: Cluster generation and network component insertion. , 2011, , .		16
9	Buffer planning as an Integral part of floorplanning with consideration of routing congestion. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2005, 24, 609-621.	1.9	14
10	A buffer planning algorithm based on dead space redistribution. , 2003, , .		13
11	High throughput hardware architecture for accurate semi-global matching. The Integration VLSI Journal, 2019, 65, 417-427.	1.3	13
12	An integrated floorplanning with an efficient buffer planning algorithm. , 2003, , .		12
13	Floorplanning and Topology Synthesis for Application-Specific Network-on-Chips. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2013, E96.A, 1174-1184.	0.2	12
14	Fault tolerance in memristive crossbar-based neuromorphic computing systems. The Integration VLSI Journal, 2020, 70, 70-79.	1.3	12
15	Lagrangian Relaxation Based Inter-Layer Signal Via Assignment for 3-D ICs. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 1080-1087.	0.2	12
16	Voltage-island driven floorplanning considering level-shifter positions. , 2009, , .		10
17	Security-Aware Task Scheduling Using Untrusted Components in High-Level Synthesis. IEEE Access, 2018, 6, 15663-15678.	2.6	10
18	Floorplanning and Topology Synthesis for Application-Specific Network-on-Chips with RF-Interconnect. ACM Transactions on Design Automation of Electronic Systems, 2016, 21, 1-23.	1.9	10

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19	Floorplanning driven Network-on-Chip synthesis for 3-D SoCs. , 2011, , .		9
20	Adaptive 3D-IC TSV Fault Tolerance Structure Generation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 949-960.	1.9	9
21	Integrated Optimization of Partitioning, Scheduling, and Floorplanning for Partially Dynamically Reconfigurable Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 199-212.	1.9	9
22	Generalized Fault-Tolerance Topology Generation for Application-Specific Network-on-Chips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1191-1204.	1.9	9
23	Analog Constraints Extraction based on the Signal Flow Analysis. , 0, , .		8
24	High throughput hardware architecture for accurate semi-global matching. , 2017, , .		8
25	Whitespace insertion for through-silicon via planning on 3-D SoCs. , 2010, , .		7
26	Floorplanning and topology generation for application-specific Network-on-Chip. , 2010, , .		7
27	A full layer parallel QC-LDPC decoder for WiMAX and Wi-Fi. , 2015, , .		7
28	Lagrangian relaxation based topology synthesis for Application-Specific Network-on-Chips. , 2015, , .		7
29	Low-Resource Hardware Architecture for Semi-Global Stereo Matching. , 2019, , .		7
30	Automatic implementation of arithmetic functions in high-level synthesis. , 2008, , .		6
31	Novel and efficient min cut based voltage assignment in gate level. , 2011, , .		6
32	Application-Specific Network-on-Chip synthesis with topology-aware floorplanning. , 2012, , .		6
33	Real-Time Hardware Stereo Matching Using Guided Image Filter. , 2016, , .		6
34	Voltage and Level-Shifter Assignment Driven Floorplanning. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 2990-2997.	0.2	6
35	Constraints generation for analog circuits layout. , 0, , .		5
36	A stable fixed-outline floorplanning method. , 2007, , .		5

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37	A Synthesis Method of General Floating-Point Arithmetic Units by Aligned Partition. IPSJ Transactions on System LSI Design Methodology, 2008, 1, 67-77.	0.5	5
38	Min-cut based leakage power aware scheduling in high-level synthesis. , 2013, , .		5
39	Lagrangian relaxation-based routing path allocation for application-specific network-on-chips. The Integration VLSI Journal, 2018, 61, 20-28.	1.3	5
40	Memristive Crossbar Mapping for Neuromorphic Computing Systems on 3D IC. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-19.	1.9	5
41	Cluster Generation and Network Component Insertion for Topology Synthesis of Application-Specific Network-on-Chips. IEICE Transactions on Electronics, 2012, E95.C, 534-545.	0.3	5
42	Arbitrary convex and concave rectilinear block packing based on corner block list. , 0, , .		4
43	A revisit to voltage partitioning problem. , 2010, , .		4
44	Leakage-Power-Aware Scheduling With Dual-Threshold Voltage Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3067-3079.	2.1	4
45	An Integrated Optimization Framework for Partitioning, Scheduling and Floorplanning on Partially Dynamically Reconfigurable FPGAs. , 2017, , .		4
46	Memristive Crossbar Mapping for Neuromorphic Computing Systems on 3D IC. , 2018, , .		4
47	Reconfigurable topology synthesis for application-specific NoC on partially dynamically reconfigurable systems. The Integration VLSI Journal, 2019, 65, 331-343.	1.3	4
48	Performance maximized interlayer via planning for 3D ICs. , 2007, , .		3
49	Practically scalable floorplanning with voltage island generation. , 2012, , .		3
50	Port assignment for interconnect reduction in high-level synthesis. , 2012, , .		3
51	Lagrangian relaxation based pin assignment and Through-Silicon Via planning for 3-D SoCs. , 2013, , .		3
52	Network simplex method based Multiple Voltage Scheduling in Power-efficient High-level synthesis. , 2013, , .		3
53	AutoNFT: Architecture synthesis for hardware DFT of length-of-coprime-number products. The Integration VLSI Journal, 2017, 58, 339-347.	1.3	3
54	A buffer planning algorithm based on dead space redistribution. , 0, , .		2

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55	Evaluating a bounded slice-line grid assignment in $O(n \log n)$ time. , 0, , .		2
56	A buffer planning algorithm for chip-level floorplanning. Science in China Series F: Information Sciences, 2004, 47, 763.	1.1	2
57	Fast evaluation of Bounded Slice-line Grid. Journal of Computer Science and Technology, 2004, 19, 973-980.	0.9	2
58	Floorplanning with Consideration of White Space Resource Distribution for Repeater Planning. , 0, , .		2
59	On the Number of 3-D IC Floorplan Configurations and a Solution Perturbation Method with Good Convergence. , 2006, , .		2
60	A generalized V-shaped multilevel method for large scale floorplanning. , 2009, , .		2
61	Redundant via Insertion: Removing Design Rule Conflicts and Balancing via Density. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2010, E93-A, 2372-2379.	0.2	2
62	An efficient level-shifter floorplanning method for Multi-voltage design. , 2011, , .		2
63	Mobility overlap-removal based timing-constrained scheduling. , 2011, , .		2
64	Topology-aware floorplanning for 3D application-specific Network-on-Chip synthesis. , 2013, , .		2
65	Port assignment for multiplexer and interconnection optimization. , 2013, , .		2
66	Mobility Overlap-Removal-Based Leakage Power and Register-Aware Scheduling in High-Level Synthesis. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2014, E97.A, 1709-1719.	0.2	2
67	Power-gating-aware scheduling with effective hardware resources optimization. The Integration VLSI Journal, 2018, 61, 167-177.	1.3	2
68	Security-Driven Task Scheduling for Multiprocessor System-on-Chips with Performance Constraints. , 2018, , .		2
69	Resource-Aware Multi-Layer Floorplanning for Partially Reconfigurable FPGAs. IEICE Transactions on Electronics, 2013, E96.C, 501-510.	0.3	2
70	Synthesizing A Generalized Brain-inspired Interconnection Network for Large-scale Network-on-chip Systems. , 2020, , .		2
71	Memory-aware Partitioning, Scheduling, and Floorplanning for Partially Dynamically Reconfigurable Systems. ACM Transactions on Design Automation of Electronic Systems, 2023, 28, 1-21.	1.9	2
72	A new interconnect-aware floorplan representation and its application to floorplanning targeting buffer planning. , 2005, , .		1

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73	VLSI Block Placement with Alignment Constraints based on Corner Block List. , 0, , .		1
74	A fixed-outline floorplanning method. , 2007, , .		1
75	Redundant via allocation for layer partition-based redundant via insertion. , 2009, , .		1
76	Exploration of Schedule Space by Random Walk. IPSJ Transactions on System LSI Design Methodology, 2009, 2, 30-42.	0.5	1
77	Redundant via insertion based on conflict removal. , 2010, , .		1
78	Network flow-based simultaneous retiming and slack budgeting for low power design. , 2011, , .		1
79	Floorplanning for high utilization of heterogeneous FPGAs. , 2011, , .		1
80	Floorplanning for High Utilization of Heterogeneous FPGAs. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2012, E95.A, 1529-1537.	0.2	1
81	Linear optimal one-sided single-detour algorithm for untangling twisted bus. , 2012, , .		1
82	Interconnection allocation between functional units and registers in High-Level Synthesis. , 2013, , .		1
83	Power and resource aware scheduling with multiple voltages. , 2013, , .		1
84	Irregularly shaped voltage islands generation with hazard and heal strategy. , 2015, , .		1
85	Generating Brain-Network-Inspired Topologies for Large-Scale NoCs on Monolithic 3D ICs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1552-1556.	2.2	1
86	Novel Voltage Choice and Min-Cut Based Assignment for Dual-VDD System. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2012, E95.A, 2208-2219.	0.2	1
87	Leakage Power Aware Scheduling in High-Level Synthesis. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2014, E97.A, 940-951.	0.2	1
88	Synthesizing Brain-network-inspired Interconnections for Large-scale Network-on-chips. ACM Transactions on Design Automation of Electronic Systems, 2022, 27, 1-30.	1.9	1
89	Reliability-Driven Memristive Crossbar Design in Neuromorphic Computing Systems. IEEE Transactions on Automation Science and Engineering, 2023, 20, 74-87.	3.4	1
90	Dynamic global buffer planning optimization based on detail block locating and congestion analysis. , 0, , .		0

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91	VLSI module placement with pre-placed modules and considering congestion using solution space smoothing. , 0, , .		0
92	Buffer allocation algorithm with consideration of routing congestion. , 0, , .		0
93	A buffer planning algorithm with congestion optimization. , 0, , .		0
94	Constraints generation for analog circuits layout. , 0, , .		0
95	Thermal constraints for BBL placement. , 0, , .		0
96	Performance Constrained Floorplanning Based on Partial Clustering. , 0, , .		0
97	Buffer Planning Algorithm Based on Partial Clustered Floorplanning. , 0, , .		0
98	Buffer planning based on block exchanging. , 0, , .		0
99	High-speed, pipelined implementation of squashing functions in neural networks. , 2008, , .		0
100	Convex-cost flow based redundant-via insertion with density-balance consideration. , 2009, , .		0
101	A heuristic method for module sizing under fixed-outline constraints. , 2009, , .		0
102	A dynamic programming based algorithm for post-scheduling frequency assignment in energy-efficient high-level synthesis. , 2010, , .		0
103	Post-scheduling frequency assignment for energy-efficient high-level synthesis. , 2010, , .		0
104	Through-Silicon-Via assignment for 3D ICs. , 2011, , .		0
105	Mobility overlap-removal based leakage power aware scheduling in high-level synthesis. , 2013, , .		0
106	Ant system based 3D fixed-outline floor planning. , 2014, , .		0
107	Cellular Structure-Based Fault-Tolerance TSV Configuration in 3D-IC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1196-1208.	1.9	0
108	SOLUTION SPACE SMOOTHING FOR VLSI MODULE PLACEMENT: A COMPUTATIONAL STUDY. , 2002, , .		0

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109	A New Buffer Planning Algorithm Based on Room Resizing. Lecture Notes in Computer Science, 2005, , 291-299.	1.0	0