# Eugenio Dentoni Litta

List of Publications by Year
in descending order

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Version: 2024-02-01

| 41 | 284 | 1162889 | 996849 |
|---|---|---|---|
| papers | citations | 8 | 15 |
| | | h-index | g-index |

| 42 | 42 | 42 | 357 |
|---|---|---|---|
| all docs | docs citations | times ranked | citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | Thermal Stress-Aware CMOSâ€“SRAM Partitioning in Sequential 3-D Technology. IEEE Transactions on Electron Devices, 2020, 67, 4631-4635. | 1.6 | 3 |
| 2 | Process Variation Analysis of Device Performance Using Virtual Fabrication: Methodology Demonstrated on a CMOS 14-nm FinFET Vehicle. IEEE Transactions on Electron Devices, 2020, 67, 5374-5380. | 1.6 | 9 |
| 3 | Buried Power Rail Integration With FinFETs for Ultimate CMOS Scaling. IEEE Transactions on Electron Devices, 2020, 67, 5349-5354. | 1.6 | 20 |
| 4 | Gate-Stack Engineered NBTI Improvements in Highvoltage Logic-For-Memory High-Ä¸/Metal Gate Devices. , 2019, , . | | 0 |
| 5 | Reliability Engineering Enabling Continued Logic for Memory Device Scaling. , 2019, , . | | 5 |
| 6 | CMOS integration of high-k/metal gate transistors in diffusion and gate replacement (D&GR) scheme for dynamic random access memory peripheral circuits. Japanese Journal of Applied Physics, 2018, 57, 04FB08. | 0.8 | 4 |
| 7 | First Demonstration of Vertically Stacked Gate-All-Around Highly Strained Germanium Nanowire pFETs. IEEE Transactions on Electron Devices, 2018, 65, 5145-5150. | 1.6 | 46 |
| 8 | Cost Effective FinFET Platform for Stand Alone DRAM 1Y and Beyond Memory Periphery. , 2018, , . | | 6 |
| 9 | TaN Versus TiN Metal Gate Input/Output pMOSFETs: A Low-Frequency Noise Perspective. IEEE Transactions on Electron Devices, 2018, 65, 3676-3681. | 1.6 | 8 |
| 10 | Improving the low-frequency noise performance of input/output DRAM peripheral pMOSFETs. , 2017, , . | | 2 |
| 11 | Gate stack engineering to enhance high-Î²/metal gate reliability for DRAM I/O applications. , 2017, , . | | 5 |
| 12 | Treatments for reliability improvement in thick oxides diffusion and gate replacement I/O transistors. International Journal of Materials Engineering Innovation, 2017, 8, 53. | 0.2 | 8 |
| 13 | (Invited) TmSiO as a CMOS-Compatible High-k Dielectric. ECS Transactions, 2016, 72, 79-89. | 0.3 | 0 |
| 14 | (Invited) TmSiO As a CMOS-Compatible High-k Dielectric. ECS Meeting Abstracts, 2016, , . | 0.0 | 0 |
| 15 | Step tunneling-enhanced hot-electron injection in vertical graphene base transistors. , 2015, , . | | 0 |
| 16 | Integration of TmSiO/HfO<sub>2</sub> Dielectric Stack in Sub-nm EOT High-k/Metal Gate CMOS Technology. IEEE Transactions on Electron Devices, 2015, 62, 934-939. | 1.6 | 14 |
| 17 | Characterization of high-k dielectrics using MeV elastic scattering of He ions. Nuclear Instruments & Methods in Physics Research B, 2015, 347, 52-57. | 0.6 | 2 |
| 18 | Bilayer insulator tunnel barriers for graphene-based vertical hot-electron transistors. Nanoscale, 2015, 7, 13096-13104. | 2.8 | 48 |

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|---|---|---|---|
| 19 | Threshold voltage control in TmSiO/HfO2 high-k/metal gate MOSFETs. Solid-State Electronics, 2015, 108, 24-29. | 0.8 | 4 |
| 20 | Low-Frequency Noise Characterization of Ultra-Low Equivalent-Oxide-Thickness Thulium Silicate Interfacial Layer nMOSFETs. IEEE Electron Device Letters, 2015, 36, 1355-1358. | 2.2 | 1 |
| 21 | Atomic-layer deposited thulium oxide as a passivation layer on germanium. Journal of Applied Physics, 2015, 117, . | 1.1 | 4 |
| 22 | Enhanced Channel Mobility at Sub-nm EOT by Integration of a TmSiO Interfacial Layer in HfO<sub>2</sub>/TiN High-k/Metal Gate MOSFETs. IEEE Journal of the Electron Devices Society, 2015, 3, 397-404. | 1.2 | 5 |
| 23 | Characterization of bonding surface and electrical insulation properties of inter layer dielectrics for 3D monolithic integration. , 2015, , . | | 3 |
| 24 | Recent advances in high-k dielectrics and inter layer engineering. , 2014, , . | | 3 |
| 25 | Interfacial Layer Engineering Using Thulium Silicate/Germanate for High-k/Metal Gate MOSFETs. ECS Transactions, 2014, 64, 249-260. | 0.3 | 2 |
| 26 | (Invited) Interface Engineering Routes for a Future CMOS Ge-Based Technology. ECS Transactions, 2014, 61, 73-88. | 0.3 | 2 |
| 27 | Effective workfunction control in TmSiO/HfO2 high-k/metal gate stacks. , 2014, , . | | 2 |
| 28 | Electrical characterization of thulium silicate interfacial layers for integration in high-k/metal gate CMOS technology. Solid-State Electronics, 2014, 98, 20-25. | 0.8 | 5 |
| 29 | Ultra-thin film and interface analysis of high-k dielectric materials employing Time-Of-Flight Medium Energy Ion Scattering (TOF-MEIS). Nuclear Instruments & Methods in Physics Research B, 2014, 332, 212-215. | 0.6 | 8 |
| 30 | Improved low-frequency noise for 0.3nm EOT thulium silicate interfacial layer. , 2014, , . | | 1 |
| 31 | Thulium Silicate Interfacial Layer for Scalable High-k/Metal Gate Stacks. IEEE Transactions on Electron Devices, 2013, 60, 3271-3276. | 1.6 | 19 |
| 32 | A study of low-frequency noise on high-k/metal gate stacks with in situ SiO<inf>x</inf> interfacial layer. , 2013, , . | | 2 |
| 33 | Mobility enhancement by integration of TmSiO IL in 0.65nm EOT high-k/metal gate MOSFETs. , 2013, , . | | 4 |
| 34 | Interface engineering of Ge using thulium oxide: Band line-up study. Microelectronic Engineering, 2013, 109, 204-207. | 1.1 | 9 |
| 35 | High-Deposition-Rate Atomic Layer Deposition of Thulium Oxide from TmCp<sub>3</sub>and H<sub>2</sub>O. Journal of the Electrochemical Society, 2013, 160, D538-D542. | 1.3 | 14 |
| 36 | Characterization of thulium silicate interfacial layer for high-k/metal gate MOSFETs. , 2013, , . | | 1 |

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|---|---|---|---|
| 37 | Atomic layer deposition-based interface engineering for high-k/metal gate stacks. , 2012, , . | | 1 |
| 38 | In situ SiO<inf>x</inf> interfacial layer formation for scaled ALD high-k/metal gate stacks. , 2012, , . | | 8 |
| 39 | Low-frequency noise in high-k LaLuO<inf>3</inf>/TiN MOSFETs. , 2011, , . | | 1 |
| 40 | RMG Patterning by Digital Wet Etching of Polycrystalline Metal Films. Solid State Phenomena, 0, 282, 132-138. | 0.3 | 0 |
| 41 | Challenges and Solutions of Replacement Metal Gate Patterning to Enable Gate-all-Around Device Scaling. Solid State Phenomena, 0, 314, 119-126. | 0.3 | 5 |