Guru Prasad Mishra

List of Publications by Year
in descending order

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110	1,001	471509	610901
papers	citations	17 h-index	24 g-index

110	110	110	415
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Effect of 1-D silver grated electrode on waferâ€based TOPCon c-Si solar cell. Silicon, 2022, 14, 3439-3448.	3.3	11
2	Dielectrically Modulated Hetero Channel Double Gate MOSFET as a Label Free Biosensor. Transactions on Electrical and Electronic Materials, 2022, 23, 156-163.	1.9	6
3	High-Performance Exploration of Buried Channel In_{0.53}Ga_{0.47}/InP Stepped Poly Gate MOSFET Using Asymmetric Underlap Gate Spacer. IETE Technical Review (Institution of) Tj ETQq1 1 0.784314 rgBT /Overlock	4.2	2
4	High Electric Field Sensing in Ultrathin SiOâ„‚ and Tunnel Region to Enhance GaInP/Si Dual Junction Solar Cell Performance. IEEE Sensors Journal, 2022, 22, 1273-1279.	4.7	10
5	Dual Junction GaInP/GaAs Solar Cell with Enhanced Efficiency Using Typeâ€A InP Quantum Wells. Physica Status Solidi (A) Applications and Materials Science, 2022, 219, .	1.8	7
6	Collector Engineered Bidirectional Insulated Gate Bipolar Transistor With Low Loss. IEEE Transactions on Electron Devices, 2022, 69, 1604-1607.	3.0	4
7	Hetero Channel Double Gate MOSFET for Label-free Biosensing Application. Silicon, 2022, 14, 8109-8118.	3.3	4
8	Recombination and mobility analysis of voltage preserved type-A InP multiple quantum well GaInP solar cell. Indian Journal of Physics, 2022, 96, 4119-4130.	1.8	11
9	A single gate SiGe/Si tunnel FET with rectangular HfO₂ dielectric pocket to improve I _{on}/I _{amb} current ratio. Semiconductor Science and Technology, 2022, 37, 065026.	2.0	5
10	Analysis of total ionizing dose response of optimized fin geometry workfunction modulated SOI-FinFET. Microelectronics Reliability, 2022, 134, 114549.	1.7	5
11	Design of Sub-40nm FinFET Based Label Free Biosensor. Silicon, 2022, 14, 12459-12465.	3.3	1
12	Impact of Composite Trench Stepped Hetero Channel MOSFET on Analog Performance. , 2022, , .		0
13	Impact of biomolecules position and filling area on the sensitivity of hetero stack gate MOSFET. Microelectronics Journal, 2022, 126, 105504.	2.0	7
14	Subthreshold Performance Improvement of Underlapped FinFET Using Workfunction Modulated Dual-metal Gate Technique. Silicon, 2021, 13, 1541-1548.	3.3	9
15	Junctionless Silicon Nanotube TFET for Improved DC and Radio Frequency Performance. Silicon, 2021, 13, 167-178.	3.3	15
16	Use of hetero intrinsic layer in GaAs P-I-N solar cell to improve the intermediate band performance. Materials Science and Engineering B: Solid-State Materials for Advanced Technology, 2021, 263, 114862.	3.5	5
17	Performance Evaluation of 10nm SMG FinFET with Architectural Variation towards DC/RF and Temperature Aspects. Silicon, 2021, 13, 2933-2941.	3.3	2
18	High Performance and Reliability Analysis of Implant Free Composite Channel In0.53Ga0.47As/InAs/In0.53Ga0.47As Delta-Doped MOSFET. Iranian Journal of Science and Technology - Transactions of Electrical Engineering, 2021, 45, 425-434.	2.3	3

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19	Analysis and optimization of BSF layer for highly efficient GaInP single junction solar cell. Materials Today: Proceedings, 2021, 43, 3420-3423.	1.8	13
20	Improvement in electrostatic effeciency using workfunction modulated dual metal gate FinFET. Materials Today: Proceedings, 2021, 43, 3443-3446.	1.8	6
21	Zâ€shaped gate <scp>TFET</scp> with horizontal pocket for improvement of electrostatic behavior. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2021, 34, .	1.9	13
22	Performance analysis of double-metal-gate dual-cavity dielectrically modulated-TFET as a label free biosensor. Materials Today: Proceedings, 2021, 43, 3740-3743.	1.8	1
23	A New Z-Shaped Gate Line Tunnel FET with Improved Electrostatic Performance. Iranian Journal of Science and Technology - Transactions of Electrical Engineering, 2021, 45, 1037-1050.	2.3	5
24	Linearity performance analysis of junctionless nanotube tunnel field effect transistor. Materials Today: Proceedings, 2021, 43, 3911-3915.	1.8	2
25	Influence of SET effects in low-doped double gate MOSFETs. Materials Today: Proceedings, 2021, 43, 3867-3873.	1.8	0
26	An analysis of interface trap charges to improve the reliability of a charge-plasma-based nanotube tunnel FET. Journal of Computational Electronics, 2021, 20, 1157-1168.	2.5	7
27	Ta2O5 as Tunneling Oxide for n-type Passivated c-Si CS-TOPCon Solar Cell. , 2021, , .		0
28	A low-loss variable-doped trench-insulated gate bipolar transistor with reduced on-state voltage. Semiconductor Science and Technology, 2021, 36, 075002.	2.0	2
29	Impact of bio-target location and their fill-in factor on the sensitivity of hetero channel double gate MOSFET label-free biosensor. Advances in Natural Sciences: Nanoscience and Nanotechnology, 2021, 12, 025012.	1.5	1
30	Design and Performance Assessment of Dielectrically Modulated Nanotube TFET Biosensor. IEEE Sensors Journal, 2021, 21, 16761-16769.	4.7	28
31	Electrical, Optical, and Reliability Analysis of QD-Embedded Kesterite Solar Cell. IEEE Transactions on Electron Devices, 2021, , 1-7.	3.0	10
32	Ambipolarity suppression in SiGe/Si- TFET using hetero-dielectric BOX engineering. , 2021, , .		1
33	Extensive Study on Effects of Defects in CZTS/CZTSe Quantum Dots Kesterite Solar Cells. , 2021, , .		1
34	An Extensive Simulation Based Study of Symmetrical Work Function Variation of In0.53Ga0.47As/InP DG Hetero MOSFET. , 2020, , 782-788.		0
35	Performance Assessment of a Cavity on Source ChargePlasmaTFET-based Biosensor. IEEE Sensors Journal, 2020, , 1-1.	4.7	21
36	Performance Improvement of Heterojunction Double Gate TFET with Gaussian Doping. Silicon, 2020, , 1.	3.3	7

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37	An integrated GaInP/Si dual-junction solar cell with enhanced efficiency using TOPCon technology. Applied Physics A: Materials Science and Processing, 2020, 126, 1.	2.3	18
38	Effect of Nanostructure on Carrier Transport Mechanism of III-Nitride and Kesterite Solar Cells: A Computational Analysis. IEEE Journal of the Electron Devices Society, 2020, 8, 1154-1161.	2.1	4
39	High Speed Buried Channel In0.53Ga0.47As/InP MOSFET with Corner Spacer for Low Power Applications. , 2020, , .		2
40	Sub-threshold Performance Analysis of Multi-Layered Trapezoidal Trench Gate Silicon On Nothing MOSFET for Low Power Applications. , 2020, , .		1
41	Voltage preserved GaInP single junction solar cell using type-A InP multiple quantum well structure with enhanced efficiency. Optik, 2020, 220, 165113.	2.9	13
42	Extensive Study on Effect of Pinhole Induced Electric Field in Si CS-TOPCon Solar Cell. , 2020, , .		3
43	Impact of drain doping engineering on ambipolar and high-frequency performance of ZHP line-TFET. Semiconductor Science and Technology, 2020, 35, 065003.	2.0	13
44	Design and Analysis of Dual-Metal-Gate Double-Cavity Charge-Plasma-TFET as a Label Free Biosensor. IEEE Sensors Journal, 2020, 20, 13969-13975.	4.7	51
45	An analytical model of the surface-potential-based source-pocket-doped cylindrical-gate tunnel FET with a work-function-modulated metal gate. Journal of Computational Electronics, 2020, 19, 591-602.	2.5	8
46	Preservation of open circuit voltage in a quantum dot solar cell using GaSb quantum confined superlattice. Optik, 2020, 212, 164678.	2.9	2
47	Lateral Variation-Doped Insulated Gate Bipolar Transistor for Low On-State Voltage With Low Loss. IEEE Electron Device Letters, 2020, 41, 888-891.	3.9	6
48	A Compact Analytical Model and Electrostatic Performance Investigation of Multilayer Groove Gate SOI-MOSFET. , 2020, , 753-760.		0
49	Incorporation of Different Quantum Superlattices in a Single Junction GaAs Solar Cell: A Comparative Study. , 2020, , 796-802.		0
50	Design and modelling of InGaP/GaSb tandem cell with embedded 1D GaAs quantum superlattice. IET Circuits, Devices and Systems, 2020, 14, 471-476.	1.4	2
51	Linearity/intermodulation distortion analysis of tunneling and thermionic emission mechanisms; design proposal and high frequency investigation. Semiconductor Science and Technology, 2020, 35, 105021.	2.0	0
52	Use of InGaAs/GaSb Quantum Ratchet in p-i-n GaAs Solar Cell for Voltage Preservation and Higher Conversion Efficiency. IEEE Transactions on Electron Devices, 2019, 66, 153-159.	3.0	15
53	Influence of Structural Parameters on the Behavior of an Asymmetric Linearly Graded Workfunction Trapezoidal Gate SOI MOSFET. Journal of Electronic Materials, 2019, 48, 6607-6616.	2.2	4
54	Effect of impact ionization on the performance of quantum ratchet embedded intermediate band solar cell: An extensive simulation study. Optik, 2019, 199, 163382.	2.9	5

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55	Heterogeneous Dielectric gate technique to enhance the performance of InGaAs/InP trench MOSFET. Materials Today: Proceedings, 2019, 11, 985-990.	1.8	1
56	Work-function modulated hetero gate charge plasma TFET to enhance the device performance. , 2019, , .		13
57	Extensive analysis of band alignment engineering on the open circuit voltage performance of a GaAs/GaSb hetero structure solar cell. , 2019, , .		0
58	Impact of Work-Function Modulation and Hetero Gate Engineering on Linearity and RF Performance of Charge Plasma TFET. International Journal of Nanoscience, 2019, , .	0.7	1
59	Inner-Gate-Engineered GAA MOSFET to Enhance the Electrostatic Integrity. Nano, 2019, 14, 1950128.	1.0	24
60	Electrostatic and radio frequency performance investigation of Î´-doped In0.53Ga0.47As/InP stepped poly gate metal oxide semiconductor field effect transistor. Journal of Micromechanics and Microengineering, 2019, 29, 084001.	2.6	3
61	Grooved-gate silicon-on-nothing (SON) MOSFET: evidence for suppressing SCEs. Nanomaterials and Energy, 2019, 8, 159-166.	0.2	1
62	Variation of source gate workfunction on the performance of dual material gate rectangular recessed channel SOIâ€MOSFET. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2019, 32, e2487.	1.9	12
63	Efficient Use of Low-Bandgap GaAs/GaSb to Convert More than 50% of Solar Radiation into Electrical Energy: A Numerical Approach. Journal of Electronic Materials, 2019, 48, 560-570.	2.2	10
64	Impact of Underlap Engineering on Stepped Poly Gate In0.53Ga0.47As/InP Heterostructure Metal Oxide Semiconductor Field Effect Transistor for Better Analog Performance. Journal of Nanoelectronics and Optoelectronics, 2019, 14, 923-931.	0.5	2
65	Use of ratchet band in a quantum dot embedded intermediate band solar cell to enrich the photo response. Materials Letters, 2018, 218, 139-141.	2.6	13
66	Current switching ratio optimization using dual pocket doping engineering. Superlattices and Microstructures, 2018, 113, 791-798.	3.1	1
67	Improved Switching Speed of a CMOS Inverter Using Work-Function Modulation Engineering. IEEE Transactions on Electron Devices, 2018, 65, 2422-2429.	3.0	24
68	Design and modeling of an SJ infrared solar cell approaching upper limit of theoretical efficiency. International Journal of Modern Physics B, 2018, 32, 1850014.	2.0	9
69	Impact of source pocket doping on RF and linearity performance of a cylindrical gate tunnel FET. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2018, 31, e2283.	1.9	10
70	An Extensive Simulation Study of Gaussian Drain Doped Heterojunction Double Gate TFET. , 2018, , .		3
71	Ambipolar Performance Improvement of Dual Material TFET Using Drain Underlap Engineering. , 2018, , .		5
72	Stepped Poly Gate In0.53Ga0.47As/InP MOSHFET to Enhance the Device Performance. , 2018, , .		0

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73	Impact of source-pocket engineering on device performance of dielectric modulated tunnel FET. Superlattices and Microstructures, 2018, 124, 131-138.	3.1	18
74	Impact of metal grain work function variability on ferroelectric insulation based GAA MOSFET. Micro and Nano Letters, 2018, 13, 1378-1381.	1.3	7
75	Analytical modelling of workâ€function modulated deltaâ€doped TFET to improve analogue performance. IET Circuits, Devices and Systems, 2018, 12, 374-381.	1.4	0
76	Impact of hetero-dielectric engineering on the performance of single gate tunnel FET. , 2018, , .		2
77	Effect of underlap length variation on DC/RF performance of dual material cylindrical MOS. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2017, 30, e2175.	1.9	4
78	Dual delta tunnel FET: An energy efficient switch with improved current switching ratio and steeper subthreshold slope. Superlattices and Microstructures, 2017, 107, 219-227.	3.1	3
79	Investigation of electrostatic performance for a conical surrounding gate MOSFET with linearly modulated work-function. Superlattices and Microstructures, 2017, 101, 152-159.	3.1	11
80	Effective use of spectrum by an ARC less dual junction solar cell to achieve higher efficiency: A simulation study. Superlattices and Microstructures, 2017, 109, 794-804.	3.1	20
81	Detail analysis of impact of graded tunnel diode on the performance of a dual Junction solar cell. Materials Today: Proceedings, 2017, 4, 12600-12605.	1.8	0
82	An extensive investigation of work function modulated trapezoidal recessed channel MOSFET. Superlattices and Microstructures, 2017, 111, 878-888.	3.1	12
83	A 2-D analytical model for cylindrical gate tunnel FET (CG-TFET) based on center potential. Turkish Journal of Electrical Engineering and Computer Sciences, 2017, 25, 770-782.	1.4	1
84	Conical surrounding gate MOSFET: a possibility in gate-all-around family. Advances in Natural Sciences: Nanoscience and Nanotechnology, 2016, 7, 015009.	1.5	12
85	An extensive electrostatic analysis of dual material gate all around tunnel FET (DMGAA-TFET). Advances in Natural Sciences: Nanoscience and Nanotechnology, 2016, 7, 025012.	1.5	13
86	Performance analysis of SOI MOSFET with rectangular recessed channel. Advances in Natural Sciences: Nanoscience and Nanotechnology, 2016, 7, 015010.	1.5	19
87	An ARC less InGaP/GaAs DJ solar cell with hetero tunnel junction. Superlattices and Microstructures, 2016, 95, 115-127.	3.1	22
88	Improved Cut-off Frequency for Cylindrical Gate TFET Using Source Delta Doping. Procedia Technology, 2016, 25, 450-455.	1.1	21
89	Tunneling path based analytical drain current model for double gate Tunnel FET (DG-TFET). , 2016, , .		2
90	Effect of Wideband Gap Tunnel Diode and Thickness of the Window Layer on the Performance of a Dual Junction Solar Cell. Procedia Technology, 2016, 25, 684-691.	1.1	13

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91	Extensive electrostatic investigation of workfunction-modulated SOI tunnel FETs. Journal of Computational Electronics, 2016, 15, 1326-1333.	2.5	1
92	Design and modeling of an efficient metamorphic dual-junction InGaP/GaAs solar cell. Optical and Quantum Electronics, 2016, 48, 1.	3.3	11
93	Delta-doped tunnel FET (D-TFET) to improve current ratio ($$I_mathrm{ON}/I_mathrm{OFF}$$ I ON / I) Tj ETQq1 1 0.784314 rgBT /Ov	2.5	16
94	Electrostatic performance improvement of dual material cylindrical gate MOSFET using work-function modulation technique. Superlattices and Microstructures, 2016, 97, 212-220.	3.1	16
95	A new analytical drain current model of cylindrical gate silicon tunnel FET with source Î´-doping. Superlattices and Microstructures, 2016, 97, 231-241.	3.1	28
96	Design and evaluation of ARC less InGaP/GaAs DJ solar cell with InGaP tunnel junction and optimized double top BSF layer. Optik, 2016, 127, 4156-4161.	2.9	26
97	Subthreshold swing minimization of cylindrical tunnel FET using binary metal alloy gate. Superlattices and Microstructures, 2016, 91, 105-111.	3.1	18
98	An analytical Nanowire Tunnel FET (NW-TFET) model with high-k dielectric to improve the electrostatic performance. , 2015, , .		3
99	Effect of Delta Doping on the RF Performance of Nano-scale Dual Material MOSFET. Procedia Computer Science, 2015, 57, 282-287.	2.0	8
100	Impact of technology scaling on analog and RF performance of SOIâ€“TFET. Advances in Natural Sciences: Nanoscience and Nanotechnology, 2015, 6, 045005.	1.5	13
101	A 2D analytical cylindrical gate tunnel FET (CG-TFET) model: impact of shortest tunneling distance. Advances in Natural Sciences: Nanoscience and Nanotechnology, 2015, 6, 035005.	1.5	49
102	A new analytical threshold voltage model of cylindrical gate tunnel FET (CG-TFET). Superlattices and Microstructures, 2015, 86, 211-220.	3.1	49
103	Performance analysis of undoped cylindrical gate all around (GAA) MOSFET at subthreshold regime. Advances in Natural Sciences: Nanoscience and Nanotechnology, 2015, 6, 035010.	1.5	26
104	Investigation on cylindrical gate all around (GAA) to nanowire MOSFET for circuit application. Facta Universitatis - Series Electronics and Energetics, 2015, 28, 637-643.	0.9	18
105	The effect of surface modification and catalytic metal contact on methane sensing performance of nano-ZnOâ€“Si heterojunction sensor. Microelectronics Reliability, 2011, 51, 2185-2194.	1.7	31
106	Single Spin Implementation of a Low Power Cost-Effective Adder. Journal of Nanoelectronics and Optoelectronics, 2010, 5, 79-81.	0.5	0
107	Segmented Drain Engineered Tunnel Field Effect Transistor for Suppression of Ambipolarity. Silicon, 0, , 1.	3.3	3
108	Design of Junction-less Twin Source Nanotube TFET for Improved DC and RF Circuit Applications. Silicon, 0, , 1.	3.3	0

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109	Analysis of Band Alignment Engineering and Interface Defects on a GaAs/GaSb Heterostructure Solar Cell. Physica Status Solidi (A) Applications and Materials Science, 0, , 2200063.	1.8	1
110	Improved Switching Current Ratio with Workfuncion Modulated Junctionless FinFET. Silicon, 0, , .	3.3	0