Andrea L Lacaita

List of Publications by Year
in descending order

315 papers	11,570 citations	36691 53 h-index	45040 94 g-index
318 all docs	318 docs citations	318 times ranked	7180 citing authors

#	Article	IF	Citations
1	A 12.9-to-15.1-GHz Digital PLL Based on a Bang-Bang Phase Detector With Adaptively Optimized Noise Shaping. IEEE Journal of Solid-State Circuits, 2022, 57, 1723-1735.	3.5	9
2	A 12.5-GHz Fractional-N Type-I Sampling PLL Achieving 58-fs Integrated Jitter. IEEE Journal of Solid-State Circuits, 2022, 57, 505-517.	3.5	19
3	Analysis and Design of 8-to-101.6-GHz Injection-Locked Frequency Divider by Five With Concurrent Dual-Path Multi-Injection Topology. IEEE Journal of Solid-State Circuits, 2022, 57, 1788-1799.	3.5	4
4	Novel Feed-Forward Technique for Digital Bang-Bang PLL to Achieve Fast Lock and Low Phase Noise. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1858-1870.	3.5	4
5	A 900-MS/s SAR-Based Time-Interleaved ADC With a Fully Programmable Interleaving Factor and On-Chip Scalable Background Calibrations. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3645-3649.	2.2	0
6	32.8 A 98.4fs-Jitter 12.9-to-15.1GHz PLL-Based LO Phase-Shifting System with Digital Background Phase-Offset Correction for Integrated Phased Arrays. , 2021, , .		5
7	32.3 A 12.9-to-15.1GHz Digital PLL Based on a Bang-Bang Phase Detector with Adaptively Optimized Noise Shaping Achieving 107.6fs Integrated Jitter. , 2021, , .		8
8	High-Density Solid-State Storage: A Long Path to Success. , 2021, , .		2
9	A 13.6-69.1GHz 5.6mW Ring-Type Injection-Locked Frequency Divider by Five with >20% Continuous Locking Range and Operation up to 101.6GHz in 28nm CMOS. , 2021, , .		3
10	Random Telegraph Noise in 3D NAND Flash Memories. Micromachines, 2021, 12, 703.	1.4	7
11	A Generalization of the Groszkowskiâ€™s Result in Differential Oscillator Topologies. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2800-2812.	3.5	3
12	Self-Biasing Dynamic Startup Circuit for Current-Biased Class-C Oscillators. IEEE Microwave and Wireless Components Letters, 2021, 31, 1075-1078.	2.0	0
13	A PLL-Based Digital Technique for Orthogonal Correction of ADC Non-Linearity. , 2021, , .		0
14	Characterization and Modeling of Current Transport in Metal/Ferroelectric/Semiconductor Tunnel Junctions. IEEE Transactions on Electron Devices, 2020, 67, 3729-3735.	1.6	11
15	A 66-fs-rms Jitter 12.8-to-15.2-GHz Fractional-*N* Bangâ€"Bang PLL With Digital Frequency-Error Recovery for Fast Locking. IEEE Journal of Solid-State Circuits, 2020, 55, 3349-3361.	3.5	44
16	Variability Effects in Nanowire and Macaroni MOSFETsâ€"Part II: Random Telegraph Noise. IEEE Transactions on Electron Devices, 2020, 67, 1492-1497.	1.6	5
17	Variability Effects in Nanowire and Macaroni MOSFETsâ€"Part I: Random Dopant Fluctuations. IEEE Transactions on Electron Devices, 2020, 67, 1485-1491.	1.6	14
18	17.5 A 12.5GHz Fractional-N Type-I Sampling PLL Achieving 58fs Integrated Jitter. , 2020, , .		23

#	Article	IF	Citations
19	17.2 A 66fs$_{rms}$Jitter 12.8-to-15.2GHz Fractional-N Bang-Bang PLL with Digital Frequency-Error Recovery for Fast Locking. , 2020, , .		7
20	Random Telegraph Noise in Flash Memories. , 2020, , 201-227.		0
21	A 1.6-to-3.0-GHz Fractional-N MDLL with a Digital-to-Time Converter Range-Reduction Technique Achieving 397fs Jitter at 2.5-mW Power. , 2019, , .		7
22	A 30-GHz Digital Sub-Sampling Fractional-N PLL With ∽238.6-dB Jitter-Power Figure of Merit in 65-nm LP CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 3493-3502.	3.5	23
23	A 1.6-to-3.0-GHz Fractional-${N}$ MDLL With a Digital-to-Time Converter Range-Reduction Technique Achieving 397-fs Jitter at 2.5-mW Power. IEEE Journal of Solid-State Circuits, 2019, 54, 3149-3160.	3.5	30
24	Time-Variant Modeling and Analysis of Multiplying Delay-Locked Loops. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3775-3785.	3.5	13
25	16.7 A 30GHz Digital Sub-Sampling Fractional-N PLL with 198fs<inf>rms</inf> Jitter in 65nm LP CMOS. , 2019, , .		7
26	Compact modeling of GIDL-assisted erase in 3-D NAND Flash strings. Journal of Computational Electronics, 2019, 18, 561-568.	1.3	13
27	Current Transport in Polysilicon-channel GAA MOSFETs: A Modeling Perspective. , 2019, , .		3
28	A Novel Single-Inductor Injection-Locked Frequency Divider by Three With Dual-Injection Secondary Locking. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1737-1745.	3.5	10
29	High Scale-Factor Stability Frequency-Modulated MEMS Gyroscope: 3-Axis Sensor and Integrated Electronics Design. IEEE Transactions on Industrial Electronics, 2018, 65, 5040-5050.	5.2	48
30	Efficient Behavioral Simulation of Charge-Pump Phase-Locked Loops. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1968-1980.	3.5	12
31	A Single-Inductor Two-Step-Mixing Injection-Locked Frequency Divider by Four with Concurrent Tail-Injection. , 2018, , .		1
32	Random Dopant Fluctuation and Random Telegraph Noise in Nanowire and Macaroni MOSFETs. , 2018, , .		4
33	A Background Calibration Technique to Control the Bandwidth of Digital PLLs. IEEE Journal of Solid-State Circuits, 2018, 53, 3243-3255.	3.5	14
34	A Low-Power and Wide-Locking-Range Injection-Locked Frequency Divider by Three with Dual-Injection Divide-by-Two Technique. , 2018, , .		4
35	Investigation and Compact Modeling of the Time Dynamics of the GIDL-Assisted Increase of the String Potential in 3-D NAND Flash Arrays. IEEE Transactions on Electron Devices, 2018, 65, 2804-2811.	1.6	23
36	Optimization of low-power oscillator topology for frequency modulated MEMS inertial sensors. , 2018, , .		5

#	Article	IF	Citations
37	Impact of CMOS Scaling on Switched-Capacitor Power Amplifiers. , 2018, , .		4
38	Characterization and Modeling of Temperature Effects in 3-D NAND Flash Arraysâ€"Part II: Random Telegraph Noise. IEEE Transactions on Electron Devices, 2018, 65, 3207-3213.	1.6	25
39	Characterization and Modeling of Temperature Effects in 3-D NAND Flash Arraysâ€"Part I: Polysilicon-Induced Variability. IEEE Transactions on Electron Devices, 2018, 65, 3199-3206.	1.6	52
40	Powerâ€jitter tradeâ€off analysis in digitalâ€toâ€time converters. Electronics Letters, 2017, 53, 306-308.	0.5	17
41	A 160 ÂµA, 8 mdps/<inf>â^š</inf>Hz frequency-modulated MEMS yaw gyroscope. , 2017, , .		9
42	Reviewing the Evolution of the NAND Flash Technology. Proceedings of the IEEE, 2017, 105, 1609-1633.	16.4	135
43	Temperature activation of the string current and its variability in 3-D NAND flash arrays. , 2017, , .		17
44	A novel segmentation scheme for DTC-based Î"Î£ fractional-N PLL. , 2017, , .		1
45	The First Frequency-Modulated (FM) Pitch Gyroscope. Proceedings (mdpi), 2017, 1, 393.	0.2	5
46	Impact of temperature on the amplitude of RTN fluctuations in 3-D NAND flash cells. , 2017, , .		12
47	Reliability of NAND Flash Memories: Planar Cells and Emerging Issues in 3D Devices. Computers, 2017, 6, 16.	2.1	66
48	A step ahead toward a new microscopic picture for charge trapping/detrapping in flash memories. , 2016, , .		4
49	A 70.7-dB SNDR 100-kS/s 14-b SAR ADC with attenuation capacitance calibration in 0.35-Âµm CMOS. Analog Integrated Circuits and Signal Processing, 2016, 89, 357-371.	0.9	7
50	Bipolar switching in chalcogenide phase change memory. Scientific Reports, 2016, 6, 29162.	1.6	59
51	Bipolar-switching operated phase change memory (PCM) for improved high-temperature reliability. , 2016, , .		0
52	Investigation of the Program Operation of NAND Flash Cells With a Single-Electron Resolution. IEEE Transactions on Electron Devices, 2016, 63, 2360-2366.	1.6	3
53	A 64-Channel 965- <inline-formula> <tex-math notation="LaTeX">$\muext{W}$</tex-math> </inline-formula> Neural Recording SoC With UWB Wireless Transmission in 130-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 528-532.	2.2	18
54	A single-electron analysis of NAND flash memory programming. , 2015, , .		9

#	Article	IF	Citations
55	A Tool for the Assisted Design of Charge Redistribution SAR ADCs. , 2015, , .		6
56	Universal Thermoelectric Characteristic in Phase Change Memories. , 2015, , .		0
57	A low-noise sub-500µW lorentz force based integrated magnetic field sensing system. , 2015, , .		0
58	Simple model for the performance of realistic AMR magnetic field sensors. , 2015, , .		4
59	Random Telegraph Noise-Induced Sensitivity of Data Retention to Cell Position in the Programmed Distribution of NAND Flash Memory Arrays. IEEE Electron Device Letters, 2015, 36, 678-680.	2.2	3
60	Fundamental Power Limits of SAR and Î"Î£ Analog-to-Digital Converters. , 2015, , .		1
61	Impact of the array background pattern on cycling-induced threshold-voltage instabilities in nanoscale NAND Flash memories. Solid-State Electronics, 2015, 113, 138-143.	0.8	0
62	Investigation of the Turn-ON of T-RAM Cells Under Transient Conditions. IEEE Transactions on Electron Devices, 2015, 62, 1170-1176.	1.6	10
63	Fitting Cells Into a Narrow <inline-formula> <tex-math notation="LaTeX">V_{T} </tex-math></inline-formula> Interval: Physical Constraints Along the Lifetime of an Extremely Scaled NAND Flash Memory Array. IEEE Transactions on Electron Devices, 2015, 62, 1491-1497.	1.6	16
64	Modeling of Dynamic Operation of T-RAM Cells. IEEE Transactions on Electron Devices, 2015, 62, 1905-1911.	1.6	10
65	First Detection of Single-Electron Charging of the Floating Gate of NAND Flash Memory Cells. IEEE Electron Device Letters, 2015, 36, 132-134.	2.2	9
66	Cell-to-Cell and Cycle-to-Cycle Retention Statistics in Phase-Change Memory Arrays. IEEE Transactions on Electron Devices, 2015, 62, 2205-2211.	1.6	9
67	A Sub-400-nT/<inline-formula> <tex-math notation="LaTeX">$sqrt {ext {Hz}}$ </tex-math></inline-formula>, 775-<inline-formula> <tex-math notation="LaTeX">$mu ext{W}$ </tex-math></inline-formula>, Multi-Loop MEMS Magnetometer With Integrated Readout Electronics. Journal of Microelectromechanical Systems, 2015, 24, 1938-1950.	1.7	24
68	A 1.7 GHz Fractional-N Frequency Synthesizer Based on a Multiplying Delay-Locked Loop. IEEE Journal of Solid-State Circuits, 2015, 50, 2678-2691.	3.5	49
69	Impact of Thermoelectric Effects on Phase Change Memory Characteristics. IEEE Transactions on Electron Devices, 2015, 62, 3264-3271.	1.6	22
70	Revisiting Charge Trapping/Detrapping in Flash Memories From a Discrete and Statistical Standpointâ€"Part II: On-Field Operation and Distributed-Cycling Effects. IEEE Transactions on Electron Devices, 2014, 61, 2811-2819.	1.6	19
71	Cycling-induced threshold-voltage instabilities in nanoscale NAND flash memories: Sensitivity to the array background pattern. , 2014, , .		2
72	Data regeneration and disturb immunity of T-RAM cells. , 2014, , .		3

#	ARTICLE	IF	CITATIONS
73	A Modeling Environment for the Simulation and Design of Charge Redistribution DACs Used in SAR ADCs. , 2014, , .		3
74	Reliability investigation of T-RAM cells for DRAM applications. , 2014, , .		5
75	Reset-induced variability of retention characteristics in phase change memory (PCM). , 2014, , .		4
76	Revisiting Charge Trapping/Detrapping in Flash Memories From a Discrete and Statistical Standpointâ€"Part I: (V_{T}) Instabilities. IEEE Transactions on Electron Devices, 2014, 61, 2802-2810.	1.6	22
77	Optimization metrics for Phase Change Memory (PCM) cell architectures. , 2014, , .		39
78	High Quality Wafer-scale CVD Graphene on Molybdenum Thin Film for Sensing Application. Procedia Engineering, 2014, 87, 1501-1504.	1.2	17
79	A new spectral approach to modeling charge trapping/detrapping in NAND Flash memories. , 2014, , .		8
80	Working Principles of a DRAM Cell Based on Gated-Thyristor Bistability. IEEE Electron Device Letters, 2014, 35, 921-923.	2.2	22
81	A 6-fJ/conversion-step 200-kSps asynchronous SAR ADC with attenuation capacitor in 130-nm CMOS. Analog Integrated Circuits and Signal Processing, 2014, 81, 181-194.	0.9	8
82	Electrical Conductivity Discontinuity at Melt in Phase Change Memory. IEEE Electron Device Letters, 2014, 35, 747-749.	2.2	15
83	2.9 A Background calibration technique to control bandwidth in digital PLLs. , 2014, , .		26
84	Analysis and optimization of a SAR ADC with attenuation capacitor. , 2014, , .		11
85	Impact of non-quasi-static effects on $1/f^3$ phase noise in a 1.9-to-2.6 GHz oscillator. , 2014, , .		1
86	21.1 A 1.7GHz MDLL-based fractional-N frequency synthesizer with 1.4ps RMS integrated jitter and 3mW power using a 1b TDC. , 2014, , .		25
87	A simulation and modeling environment for the analysis and design of charge redistribution DACs used in SAR ADCs. , 2014, , .		5
88	Dynamic Analysis of Current-Voltage Characteristics of Nanoscale Gated-Thyristors. IEEE Electron Device Letters, 2013, 34, 629-631.	2.2	12
89	A wideband voltage-biased LC oscillator with reduced flicker noise up-conversion. , 2013, , .		0
90	A Wideband Fractional-N PLL With Suppressed Charge-Pump Noise and Automatic Loop Filter Calibration. IEEE Journal of Solid-State Circuits, 2013, 48, 2419-2429.	3.5	42

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91	Suppression of Flicker Noise Up-Conversion in a 65-nm CMOS VCO in the 3.0-to-3.6 GHz Band. IEEE Journal of Solid-State Circuits, 2013, 48, 2375-2389.	3.5	75
92	Study of Cycling-Induced Parameter Variations in Phase Change Memory Cells. IEEE Electron Device Letters, 2013, 34, 882-884.	2.2	8
93	Investigation of the RTN amplitude statistics of nanoscale MOS devices by the statistical impedance field method. Journal of Computational Electronics, 2013, 12, 585-591.	1.3	0
94	Assessment of the statistical impedance field method for the analysis of the RTN amplitude in nanoscale MOS devices. , 2013, , .		0
95	A spur cancellation technique for MDLL-based frequency synthesizers. , 2013, , .		3
96	Characterization and Modeling of the Band-to-Band Current Variability of Nanoscale Device Junctions. IEEE Transactions on Electron Devices, 2013, 60, 3291-3297.	1.6	3
97	Resolving discrete emission events: A new perspective for detrapping investigation in NAND Flash memories. , 2013, , .		19
98	Accelerated reliability testing of flash memory: Accuracy and issues on a 45nm NOR technology. , 2013, , .		2
99	Background adaptive linearization of high-speed digital-to-analog Converters. , 2013, , .		0
100	New Erase Constraint for the Junction-Less Charge-Trap Memory Array in Cylindrical Geometry. IEEE Transactions on Electron Devices, 2013, 60, 2203-2208.	1.6	2
101	The race of phase change memories to nanoscale storage and applications. Microelectronic Engineering, 2013, 109, 351-356.	1.1	76
102	Accuracy and Issues of the Spectroscopic Analysis of RTN Traps in Nanoscale MOSFETs. IEEE Transactions on Electron Devices, 2013, 60, 833-839.	1.6	28
103	Reliability Characterization Issues for Nanoscale Flash Memories: A Case Study on 45-nm NOR Devices. IEEE Transactions on Device and Materials Reliability, 2013, 13, 362-369.	1.5	6
104	Analysis and Minimization of Flicker Noise Up-Conversion in Voltage-Biased Oscillators. IEEE Transactions on Microwave Theory and Techniques, 2013, 61, 2382-2394.	2.9	57
105	Investigation of the RTN Distribution of Nanoscale MOS Devices From Subthreshold to On-State. IEEE Electron Device Letters, 2013, 34, 683-685.	2.2	35
106	Reducing flicker noise up-conversion in a 65nm CMOS VCO in the 1.6 to 2.6 GHz band. Proceedings of SPIE, 2013, , .	0.8	0
107	A simulation technique to compute phase noise induced from cyclostationary noise sources in RF oscillators. Proceedings of SPIE, 2013, , .	0.8	0
108	Intrinsic retention statistics in phase change memory (PCM) arrays. , 2013, , .		5

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109	Enabling Universal Memory by Overcoming the Contradictory Speed and Stability Nature of Phase-Change Materials. Scientific Reports, 2012, 2, 360.	1.6	72
110	Evidence for an atomistic-doping induced variability of the band-to-band leakage current of nanoscale device junctions. , 2012, , .		4
111	Three-Dimensional Electrostatics- and Atomistic Doping-Induced Variability of RTN Time Constants in Nanoscale MOS Devicesâ€"Part II: Spectroscopic Implications. IEEE Transactions on Electron Devices, 2012, 59, 2495-2500.	1.6	22
112	Assessment of distributed-cycling schemes on 45nm NOR flash memory arrays. , 2012, , .		9
113	Engineering grains of Ge<inf>2</inf>Sb<inf>2</inf>Te<inf>5</inf> for realizing fast-speed, low-power, and low-drift phase-change memories with further multilevel capabilities. , 2012, , .		8
114	A 20 Mb/s Phase Modulator Based on a 3.6 GHz Digital PLL With âˆ'36 dB EVM at 5 mW Power. IEEE Journal of Solid-State Circuits, 2012, 47, 2974-2988.	3.5	81
115	A wideband fractional-N PLL with suppressed charge-pump noise and automatic loop filter calibration. , 2012, , .		5
116	Three-Dimensional Electrostatics- and Atomistic Doping-Induced Variability of RTN Time Constants in Nanoscale MOS Devicesâ€"Part I: Physical Investigation. IEEE Transactions on Electron Devices, 2012, 59, 2488-2494.	1.6	19
117	A new erase saturation issue in cylindrical junction-less charge-trap memory arrays. , 2012, , .		2
118	Characterization and modeling methodology for the evaluation of statistical variation of MOSFETs. , 2012, , .		0
119	Efficient Calculation of the Impulse Sensitivity Function in Oscillators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 628-632.	2.2	27
120	An efficient linear-time variant simulation technique of oscillator phase sensitivity function. , 2012, , .		19
121	A glitch-corrector circuit for low-spur ADPLLs. Analog Integrated Circuits and Signal Processing, 2012, 73, 201-208.	0.9	2
122	Comprehensive investigation of the impact of lateral charge migration on retention performance of planar and 3D SONOS devices. Solid-State Electronics, 2012, 74, 64-70.	0.8	45
123	Investigation of Cycling-Induced VT Instabilities in NAND Flash Cells via Compact Modeling. , 2012, , .		1
124	String Current in Decananometer nand Flash Arrays: A Compact-Modeling Investigation. IEEE Transactions on Electron Devices, 2012, 59, 2331-2337.	1.6	7
125	Flicker Noise Up-Conversion due to Harmonic Distortion in Van der Pol CMOS Oscillators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1418-1430.	3.5	40
126	A Multi-Channel Low-Power System-on-Chip for in Vivo Recording and Wireless Transmission of Neural Spikes. Journal of Low Power Electronics and Applications, 2012, 2, 211-241.	1.3	0

#	Article	IF	Citations
127	Quantum-Mechanical Charge Distribution in Cylindrical Gate-All-Around MOS Devices. IEEE Transactions on Electron Devices, 2012, 59, 1837-1843.	1.6	8
128	Electrical properties and microscopic structure of amorphous chalcogenides. , 2011, , .		0
129	Impact of atomistic doping and 3D electrostatics on the variability of RTN time constants in flash memories. , 2011, , .		11
130	Impact of lateral charge migration on the retention performance of planar and 3D SONOS devices. , 2011, , .		16
131	Low-Power Divider Retiming in a 3–4 GHz Fractional-N PLL. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 200-204.	2.2	11
132	Behavioral phase-noise analysis of charge-pump phase-locked loops. , 2011, , .		3
133	A Wideband 3.6 GHz Digital $\Sigma\Delta$ Fractional-N PLL With Phase Interpolation Divider and Digital Spur Cancellation. IEEE Journal of Solid-State Circuits, 2011, 46, 627-638.	3.5	123
134	A 2.9–4.0-GHz Fractional-N Digital PLL With Bang-Bang Phase Detector and 560-${\rm fs}_{\rm rms}$ Integrated Jitter at 4.5-mW Power. IEEE Journal of Solid-State Circuits, 2011, 46, 2745-2758.	3.5	178
135	Phase change materials in non-volatile storage. Materials Today, 2011, 14, 600-607.	8.3	146
136	Three-Dimensional Simulation of Charge-Trap Memory Programming—Part I: Average Behavior. IEEE Transactions on Electron Devices, 2011, 58, 1864-1871.	1.6	18
137	Three-Dimensional Simulation of Charge-Trap Memory Programming—Part II: Variability. IEEE Transactions on Electron Devices, 2011, 58, 1872-1878.	1.6	8
138	Semi-Analytical Model for the Transient Operation of Gate-All-Around Charge-Trap Memories. IEEE Transactions on Electron Devices, 2011, 58, 3116-3123.	1.6	29
139	Impact of Ge–Sb–Te compound engineering on the set operation performance in phase-change memories. Solid-State Electronics, 2011, 58, 11-16.	0.8	24
140	A wireless microsystem with digital data compression for neural spike recording. Microelectronic Engineering, 2011, 88, 1672-1675.	1.1	4
141	Investigation of the programming accuracy of a double-verify ISPP algorithm for nanoscale NAND Flash memories. , 2011, , .		8
142	Multipath adaptive cancellation of divider non-linearity in fractional-N PLLs. , 2011, , .		15
143	A 2.9-to-4.0GHz fractional-N digital PLL with bang-bang phase detector and 560fs<inf>rms</inf> integrated jitter at 4.5mW power. , 2011, , .		42
144	Fundamental Limitations to the Width of the Programmed <formula formulatype="inline"><tex Notation="TeX"> V_{T}</tex></formula> Distribution of <emphasis emphasistype="smcaps">nor</emphasis> Flash Memories. IEEE Transactions on Electron Devices, 2010, 57, 1761-1767.	1.6	14

#	Article	IF	Citations
145	A New Transient Model for Recovery and Relaxation Oscillations in Phase-Change Memories. IEEE Transactions on Electron Devices, 2010, 57, 1838-1845.	1.6	19
146	Comprehensive Investigation of Statistical Effects in Nitride Memoriesâ€"Part I: Physics-Based Modeling. IEEE Transactions on Electron Devices, 2010, 57, 2116-2123.	1.6	25
147	Comprehensive Investigation of Statistical Effects in Nitride Memoriesâ€"Part II: Scaling Analysis and Impact on Device Performance. IEEE Transactions on Electron Devices, 2010, 57, 2124-2131.	1.6	14
148	Statistics of Resistance Drift Due to Structural Relaxation in Phase-Change Memory Arrays. IEEE Transactions on Electron Devices, 2010, 57, 2690-2696.	1.6	75
149	Transient Simulation of Delay and Switching Effects in Phase-Change Memories. IEEE Transactions on Electron Devices, 2010, 57, 3257-3264.	1.6	22
150	Size-dependent Temperature Instability in NiOâ€"based Resistive Switching Memory. Materials Research Society Symposia Proceedings, 2010, 1250, 1.	0.1	1
151	3D Monte Carlo simulation of the programming dynamics and their statistical variability in nanoscale charge-trap memories. , 2010, , .		13
152	Investigation of the ISPP dynamics and of the programming efficiency of charge-trap memories. , 2010, , .		3
153	Temperature- and time-dependent conduction controlled by activation energy in PCM. , 2010, , .		12
154	A multi-channel low-power system-on-chip for single-unit recording and narrowband wireless transmission of neural signal. , 2010, 2010, 1555-60.		19
155	Trade-off between data retention and reset in NiO RRAMS. , 2010, , .		11
156	Time-to-Digital Converter for Frequency Synthesis Based on a Digital Bang-Bang DLL. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 548-555.	3.5	55
157	Time-to-digital converter with 3-ps resolution and digital linearization algorithm. , 2010, , .		19
158	A multi-channel low-power IC for neural spike recording with data compression and narrowband 400-MHz MC-FSK wireless transmission. , 2010, , .		26
159	Random telegraph signal noise in phase change memory devices. , 2010, , .		15
160	Size-Dependent Retention Time in NiO-Based Resistive-Switching Memories. IEEE Electron Device Letters, 2010, 31, 353-355.	2.2	115
161	Folding of Phase Noise Spectra in Charge-Pump Phase-Locked Loops Induced by Frequency Division. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 671-675.	2.2	16
162	Incomplete Filament Crystallization During Set Operation in PCM Cells. IEEE Electron Device Letters, 2010, 31, 341-343.	2.2	11

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163	Impact of material composition on the write performance of phase-change memory devices. , 2010, , .		8
164	Impact of Control-Gate and Floating-Gate Design on the Electron-Injection Spread of Decananometer nand Flash Memories. IEEE Electron Device Letters, 2010, , .	2.2	6
165	Variability effects on the V<inf>T</inf> distribution of nanoscale NAND Flash memories. , 2010, , .		12
166	Investigation of the threshold voltage instability after distributed cycling in nanoscale NAND Flash memory arrays. , 2010, , .		29
167	Reliability constraints for TANOS memories due to alumina trapping and leakage. , 2010, , .		11
168	Granular electron injection and random telegraph noise impact on the programming accuracy of NOR Flash memories. , 2009, , .		5
169	Filament Conduction and Reset Mechanism in NiO-Based Resistive-Switching Memory (RRAM) Devices. IEEE Transactions on Electron Devices, 2009, 56, 186-192.	1.6	314
170	Self-Accelerated Thermal Dissolution Model for Reset Programming in Unipolar Resistive-Switching Memory (RRAM) Devices. IEEE Transactions on Electron Devices, 2009, 56, 193-200.	1.6	345
171	Study of Multilevel Programming in Programmable Metallization Cell (PMC) Memory. IEEE Transactions on Electron Devices, 2009, 56, 1040-1047.	1.6	291
172	Reliability Impact of Chalcogenide-Structure Relaxation in Phase-Change Memory (PCM) Cellsâ€"Part I: Experimental Study. IEEE Transactions on Electron Devices, 2009, 56, 1070-1077.	1.6	149
173	Reliability Impact of Chalcogenide-Structure Relaxation in Phase-Change Memory (PCM) Cellsâ€"Part II: Physics-Based Modeling. IEEE Transactions on Electron Devices, 2009, 56, 1078-1085.	1.6	63
174	Unified mechanisms for structural relaxation and crystallization in phase-change memory devices. Microelectronic Engineering, 2009, 86, 1942-1945.	1.1	36
175	Noise Analysis and Minimization in Bang-Bang Digital PLLs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 835-839.	2.2	90
176	A glitch-corrector circuit for low-spur ADPLLs. , 2009, , .		4
177	Statistical and scaling behavior of structural relaxation effects in phase-change memory (PCM) devices. Reliability Physics Symposium, 2009 IEEE International, 2009, , .	0.0	19
178	Distributed-Poole-Frenkel modeling of anomalous resistance scaling and fluctuations in phase-change memory (PCM) devices. , 2009, , .		30
179	Random Telegraph Noise Effect on the Programmed Threshold-Voltage Distribution of Flash Memories. IEEE Electron Device Letters, 2009, 30, 984-986.	2.2	85
180	Explanation of programming distributions in phase-change memory arrays based on crystallization time statistics. Solid-State Electronics, 2008, 52, 584-590.	0.8	15

#	Article	IF	Citations
181	Phaseâ€change memories. Physica Status Solidi (A) Applications and Materials Science, 2008, 205, 2281-2297.	0.8	129
182	Status and challenges of phase change memory modeling. Solid-State Electronics, 2008, 52, 1443-1451.	0.8	18
183	Modeling of Programming and Read Performance in Phase-Change Memoriesâ€"Part I: Cell Optimization and Scaling. IEEE Transactions on Electron Devices, 2008, 55, 506-514.	1.6	109
184	Modeling of Programming and Read Performance in Phase-Change Memoriesâ€"Part II: Program Disturb and Mixed-Scaling Approach. IEEE Transactions on Electron Devices, 2008, 55, 515-522.	1.6	44
185	Statistical Model for Random Telegraph Noise in Flash Memories. IEEE Transactions on Electron Devices, 2008, 55, 388-395.	1.6	113
186	Low-Power Signal Component Separator for a 64-QAM 802.11 LINC Transmitter. IEEE Journal of Solid-State Circuits, 2008, 43, 1274-1286.	3.5	14
187	Transient effects of delay, switching and recovery in phase change memory (PCM) devices. , 2008, , .		23
188	Evidence for threshold switching in the set process of NiO-based RRAM and physical modeling for set, reset, retention and disturb prediction. , 2008, , .		36
189	Threshold switching and phase transition numerical models for phase change memory simulations. Journal of Applied Physics, 2008, 103, .	1.1	217
190	Scaling trends for random telegraph noise in deca-nanometer Flash memories. , 2008, , .		61
191	Voltage-Controlled Relaxation Oscillations in Phase-Change Memory Devices. IEEE Electron Device Letters, 2008, 29, 568-570.	2.2	23
192	Recent Advances on the Modeling of Phase Change Materials and Devices. Materials Research Society Symposia Proceedings, 2008, 1072, 1.	0.1	0
193	A new physics-based model for TANOS memories program/erase. , 2008, , .		10
194	Physical mechanism and temperature acceleration of relaxation effects in phase-change memory cells. , 2008, , .		25
195	A Reliable Technique for Experimental Evaluation of Crystallization Activation Energy in PCMs. IEEE Electron Device Letters, 2008, 29, 41-43.	2.2	24
196	Temperature acceleration of structural relaxation in amorphous Ge2Sb2Te5. Applied Physics Letters, 2008, 92, .	1.5	81
197	Modeling and Simulation of Conduction Characteristics and Programming Operation in Nanoscaled Phase-Change Memory Cells. Journal of Computational and Theoretical Nanoscience, 2008, 5, 1183-1191.	0.4	3
198	Statistical Investigation of Random Telegraph Noise ID Instabilities in Flash Cells at Different Initial Trap-filling Conditions. , 2007, , .		15

#	Article	IF	Citations
199	First evidence for injection statistics accuracy limitations in NAND Flash constant-current Fowler-Nordheim programming. , 2007, , .		50
200	Physical interpretation, modeling and impact on phase change memory (PCM) reliability of resistance drift due to chalcogenide structural relaxation. , 2007, , .		94
201	Statistical analysis and modeling of programming and retention in PCM arrays. , 2007, , .		33
202	Quantization Effects in All-Digital Phase-Locked Loops. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 1120-1124.	2.2	33
203	Conductive-filament switching analysis and self-accelerated thermal dissolution model for reset in NiO-based RRAM. , 2007, , .		95
204	Experimental Study of Data Retention in Nitride Memories by Temperature and Field Acceleration. IEEE Electron Device Letters, 2007, 28, 628-630.	2.2	17
205	Reliability issues and scaling projections for phase change non volatile memories. , 2007, , .		6
206	Anomalous Cells With Low Reset Resistance in Phase-Change-Memory Arrays. IEEE Electron Device Letters, 2007, 28, 865-867.	2.2	17
207	A Physics-Based Crystallization Model for Retention in Phase-Change Memories. , 2007, , .		9
208	An integrated low-noise multichannel system for neural signals amplification. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2007, , .	0.0	5
209	Status and challenges of PCM modeling. , 2007, , .		2
210	Comparison of Modeling Approaches for the Capacitanceâ€"Voltage and Currentâ€"Voltage Characteristics of Advanced Gate Stacks. IEEE Transactions on Electron Devices, 2007, 54, 106-114.	1.6	27
211	Recovery and Drift Dynamics of Resistance and Threshold Voltages in Phase-Change Memories. IEEE Transactions on Electron Devices, 2007, 54, 308-315.	1.6	223
212	Analytical Modeling of Chalcogenide Crystallization for PCM Data-Retention Extrapolation. IEEE Transactions on Electron Devices, 2007, 54, 2769-2777.	1.6	70
213	Silicon nanocrystal memories: a status update. Journal of Nanoscience and Nanotechnology, 2007, 7, 193-205.	0.9	1
214	Low-power CMOS IEEE 802.11a/g Signal Separator for Outphasing Transmitter. , 2006, , .		3
215	Defects spectroscopy in SiO2 by statistical random telegraph noise analysis. , 2006, , .		27
216	5-GHz Oscillator Array With Reduced Flicker Up-Conversion in 0.13-<tex>$muhboxm$</tex>CMOS. IEEE Journal of Solid-State Circuits, 2006, 41, 2457-2467.	3.5	30

#	Article	IF	Citations
217	Wireless multi-standard terminals: system analysis and design of a reconfigurable RF front-end. IEEE Circuits and Systems Magazine, 2006, 6, 38-59.	2.6	71
218	Extraction of the floating-gate capacitive couplings for drain turn-on estimation in discrete-trap memories. Microelectronic Engineering, 2006, 83, 319-322.	1.1	4
219	Phase change memories: State-of-the-art, challenges and perspectives. Solid-State Electronics, 2006, 50, 24-31.	0.8	271
220	Characterization of transient currents in HfO2 capacitors in the short timescale. Microelectronic Engineering, 2006, 83, 1927-1930.	1.1	1
221	Intrinsic Data Retention in Nanoscaled Phase-Change Memories—Part II: Statistical Analysis and Prediction of Failure Time. IEEE Transactions on Electron Devices, 2006, 53, 3040-3046.	1.6	69
222	Intrinsic Data Retention in Nanoscaled Phase-Change Memories—Part I: Monte Carlo Model for Crystallization and Percolation. IEEE Transactions on Electron Devices, 2006, 53, 3032-3039.	1.6	91
223	Electrical characterization of anomalous cells in phase change memory arrays. , 2006, , .		15
224	Temperature dependence of transient and steady-state gate currents in HfO2 capacitors. Applied Physics Letters, 2006, 89, 103504.	1.5	7
225	Low-Power All-Analog Component Separator for an 802.11a/g LINC Transmitter. , 2006, , .		3
226	Transient currents in HfO2 and their impact on circuit and memory applications. , 2006, , .		1
227	Edge and percolation effects on VT window in nanocrystal memories. Microelectronic Engineering, 2005, 80, 186-189.	1.1	5
228	Quantum-corrected drift-diffusion models for transport in semiconductor devices. Journal of Computational Physics, 2005, 204, 533-561.	1.9	91
229	Recent developments on Flash memory reliability. Microelectronic Engineering, 2005, 80, 321-328.	1.1	29
230	Switching and programming dynamics in phase-change memory cells. Solid-State Electronics, 2005, 49, 1826-1832.	0.8	41
231	Modeling of Tunneling P/E for Nanocrystal Memories. IEEE Transactions on Electron Devices, 2005, 52, 569-576.	1.6	36
232	Optimization of Threshold Voltage Window Under Tunneling Program/Erase in Nanocrystal Memories. IEEE Transactions on Electron Devices, 2005, 52, 2473-2481.	1.6	17
233	Parasitic reset in the programming transient of PCMs. IEEE Electron Device Letters, 2005, 26, 799-801.	2.2	54
234	A 15-GHz broad-band /spl divide/2 frequency divider in 0.13-/spl mu/m CMOS for quadrature generation. IEEE Microwave and Wireless Components Letters, 2005, 15, 724-726.	2.0	28

#	ARTICLE	IF	CITATIONS
235	Differentially-Tuned VCO with Reduced Tuning Sensitivity and Flicker Noise Up-Conversion. Analog Integrated Circuits and Signal Processing, 2005, 42, 21-29.	0.9	6
236	Improving Floating-Gate Memory Reliability by Nanocrystal Storage and Pulsed Tunnel Programming. IEEE Transactions on Device and Materials Reliability, 2004, 4, 390-396.	1.5	6
237	A Comparative Study of Characterization Techniques for Oxide Reliability in Flash Memories. IEEE Transactions on Device and Materials Reliability, 2004, 4, 320-326.	1.5	7
238	Electronic Switching in Phase-Change Memories. IEEE Transactions on Electron Devices, 2004, 51, 452-459.	1.6	555
239	Low-field amorphous state resistance and threshold voltage drift in chalcogenide materials. IEEE Transactions on Electron Devices, 2004, 51, 714-719.	1.6	329
240	Impact of Correlated Generation of Oxide Defects on SILC and Breakdown Distributions. IEEE Transactions on Electron Devices, 2004, 51, 1281-1287.	1.6	9
241	Defect Generation Statistics in Thin Gate Oxides. IEEE Transactions on Electron Devices, 2004, 51, 1288-1295.	1.6	16
242	Optimization of the Nonoverlap Length in Decanano MOS Devices with 2-D QM Simulations. IEEE Transactions on Electron Devices, 2004, 51, 1849-1855.	1.6	10
243	Study of nanocrystal memory reliability by CAST structures. Solid-State Electronics, 2004, 48, 1497-1502.	0.8	8
244	A 13.5-mW 5-GHz Frequency Synthesizer With Dynamic-Logic Frequency Divider. IEEE Journal of Solid-State Circuits, 2004, 39, 378-383.	3.5	181
245	Phase noise in digital frequency dividers. IEEE Journal of Solid-State Circuits, 2004, 39, 775-784.	3.5	98
246	Reliability Study of Phase-Change Nonvolatile Memories. IEEE Transactions on Device and Materials Reliability, 2004, 4, 422-427.	1.5	232
247	Analysis of Phase Distribution in Phase-Change Nonvolatile Memories. IEEE Electron Device Letters, 2004, 25, 507-509.	2.2	112
248	Electronic Switching Effect and Phase-Change Transition in Chalcogenide Materials. IEEE Electron Device Letters, 2004, 25, 684-686.	2.2	120
249	Frequency dependence on bias current in 5 GHz CMOS VCOs: impact on tuning range and flicker noise upconversion. IEEE Journal of Solid-State Circuits, 2002, 37, 1003-1011.	3.5	256
250	Equivalent cell approach for extraction of the SILC distribution in flash EEPROM cells. IEEE Electron Device Letters, 2002, 23, 40-42.	2.2	26
251	Two-dimensional quantum effects in nanoscale MOSFETs. IEEE Transactions on Electron Devices, 2002, 49, 25-31.	1.6	36
252	Statistical profiling of SILC spot in flash memories. IEEE Transactions on Electron Devices, 2002, 49, 1723-1728.	1.6	11

#	Article	IF	Citations
253	A statistical model for SILC in flash memories. IEEE Transactions on Electron Devices, 2002, 49, 1955-1961.	1.6	59
254	Modeling of stress-induced leakage current and impact ionization in MOS devices. Solid-State Electronics, 2002, 46, 417-422.	0.8	4
255	Simulation of polysilicon quantization and its effect on n- and p-MOSFET performance. Solid-State Electronics, 2002, 46, 423-428.	0.8	6
256	Modeling of anomalous SILC in flash memories based on tunneling at multiple defects. Solid-State Electronics, 2002, 46, 1749-1756.	0.8	14
257	A 2-V 2.5-GHz-104-dBc/Hz at 100 kHz fully integrated VCO with wide-band low-noise automatic amplitude control loop. IEEE Journal of Solid-State Circuits, 2001, 36, 611-619.	3.5	56
258	A fully-integrated low-power low-noise 2.6-GHz bipolar VCO for wireless applications. IEEE Microwave and Wireless Components Letters, 2001, 11, 199-201.	2.0	11
259	An improved formula for the determination of the polysilicon doping. IEEE Electron Device Letters, 2001, 22, 281-283.	2.2	8
260	A new two-trap tunneling model for the anomalous stress-induced leakage current (SILC) in Flash memories. Microelectronic Engineering, 2001, 59, 189-195.	1.1	36
261	A recombination- and trap-assisted tunneling model for stress-induced leakage current. Solid-State Electronics, 2001, 45, 1361-1369.	0.8	10
262	Novel low-temperature C-V technique for MOS doping profile determination near the Si/SiO/sub 2/ interface. IEEE Transactions on Electron Devices, 2001, 48, 750-757.	1.6	8
263	A detailed investigation of the quantum yield experiment. IEEE Transactions on Electron Devices, 2001, 48, 1696-1702.	1.6	9
264	Different types of defects in silicon dioxide characterized by their transient behavior. Journal of Applied Physics, 2001, 89, 4189-4191.	1.1	4
265	New formulas of interconnect capacitances based on results of conformal mapping method. IEEE Transactions on Electron Devices, 2000, 47, 222-231.	1.6	99
266	Explaining the dependences of the hole and electron mobilities in Si inversion layers. IEEE Transactions on Electron Devices, 2000, 47, 718-724.	1.6	44
267	Modeling of SILC based on electron and hole tunneling. I. Transient effects. IEEE Transactions on Electron Devices, 2000, 47, 1258-1265.	1.6	91
268	Modeling of SILC based on electron and hole tunneling. II. Steady-state. IEEE Transactions on Electron Devices, 2000, 47, 1266-1272.	1.6	99
269	Polysilicon quantization effects on the electrical properties of MOS transistors. IEEE Transactions on Electron Devices, 2000, 47, 2366-2371.	1.6	40
270	On the correlation between surface roughness and inversion layer mobility in Si-MOSFETs. IEEE Electron Device Letters, 2000, 21, 34-36.	2.2	65

#	Article	IF	Citations
271	Experimental evidence for recombination-assisted leakage in thin oxides. Applied Physics Letters, 2000, 76, 1719-1721.	1.5	15
272	Effect of oxide tunneling on the measurement of MOS interface states. IEEE Electron Device Letters, 2000, 21, 405-407.	2.2	10
273	Phase noise degradation at high oscillation amplitudes in LC-tuned VCO's. IEEE Journal of Solid-State Circuits, 2000, 35, 96-99.	3.5	37
274	Analysis of space and energy distribution of stress-induced oxide traps. Microelectronics Reliability, 1999, 39, 215-219.	0.9	7
275	Monte Carlo simulation of conductance characteristics in SOI-MOSFET. Physica B: Condensed Matter, 1999, 272, 565-567.	1.3	2
276	Separation of electron and hole traps by transient current analysis. Microelectronic Engineering, 1999, 48, 151-154.	1.1	16
277	Physics and characterization of transient effects in SOI transistors. Microelectronic Engineering, 1999, 48, 319-326.	1.1	3
278	Quantum effects on the extraction of MOS oxide traps by 1/f noise measurements. IEEE Transactions on Electron Devices, 1999, 46, 1029-1035.	1.6	26
279	On surface roughness-limited mobility in highly doped n-MOSFET's. IEEE Transactions on Electron Devices, 1999, 46, 1423-1428.	1.6	56
280	MOSFET simulation with quantum effects and nonlocal mobility model. IEEE Electron Device Letters, 1999, 20, 298-300.	2.2	12
281	Experimental method for the determination of the energy distribution of stress-induced oxide traps. IEEE Electron Device Letters, 1999, 20, 106-108.	2.2	28
282	Switch-off behavior of floating-body PD SOI MOSFET's. IEEE Transactions on Electron Devices, 1998, 45, 2372-2375.	1.6	5
283	Reliable extraction of MOS interface traps from low-frequency CV measurements. IEEE Electron Device Letters, 1998, 19, 148-150.	2.2	25
284	Direct evidence of impact excitation and spatial profiling of excited Er in light emitting Si diodes. Applied Physics Letters, 1998, 73, 93-95.	1.5	54
285	Impact ionization in silicon: A microscopic view. Journal of Applied Physics, 1998, 83, 4760-4764.	1.1	5
286	Electron mobility in ULSI MOSFETs: effect of interface traps and oxide nitridation. IEEE Electron Device Letters, 1997, 18, 235-237.	2.2	11
287	Characterization and modeling of metal-resistance-semiconductor photodetectors. IEEE Transactions on Nuclear Science, 1997, 44, 957-960.	1.2	3
288	Physics and numerical simulation of single photon avalanche diodes. IEEE Transactions on Electron Devices, 1997, 44, 1931-1943.	1.6	148

#	Article	IF	Citations
289	Dead space approximation for impact ionization in silicon. Applied Physics Letters, 1996, 69, 3707-3709.	1.5	36
290	Mean gain of avalanche photodiodes in a dead space model. IEEE Transactions on Electron Devices, 1996, 43, 23-30.	1.6	55
291	On the shape of hot-carrier tails in non-local transport. Semiconductor Science and Technology, 1996, 11, 1642-1645.	1.0	1
292	Photon emission from hot electrons in silicon. Physical Review B, 1995, 52, 10993-10999.	1.1	59
293	Performance optimization of active quenching circuits for picosecond timing with single photon avalanche diodes. Review of Scientific Instruments, 1995, 66, 4289-4295.	0.6	13
294	Polarization analysis of hot-carrier light emission in silicon. Semiconductor Science and Technology, 1994, 9, 674-676.	1.0	36
295	Nanosecond single-photon timing with InGaAs/InP photodiodes. Optics Letters, 1994, 19, 846.	1.7	22
296	On the bremsstrahlung origin of hot-carrier-induced photons in silicon devices. IEEE Transactions on Electron Devices, 1993, 40, 577-582.	1.6	259
297	Subnanosecond single-photon timing with commercially available germanium photodiodes. Optics Letters, 1993, 18, 75.	1.7	18
298	Single-photon optical-time-domain reflectometer at 13 Î¼m with 5-cm resolution and high sensitivity. Optics Letters, 1993, 18, 1110.	1.7	58
299	Single-photon avalanche diode with ultrafast pulse response free from slow tails. IEEE Electron Device Letters, 1993, 14, 360-362.	2.2	35
300	Photonâ€assisted avalanche spreading in reachâ€through photodiodes. Applied Physics Letters, 1993, 62, 606-608.	1.5	50
301	Constantâ€fraction circuits for picosecond photon timing with microchannel plate photomultipliers. Review of Scientific Instruments, 1993, 64, 118-124.	0.6	12
302	Effective temperature of hot electrons: why it approaches the lattice temperature. Semiconductor Science and Technology, 1992, 7, B590-B592.	1.0	4
303	All-silicon avalanche photodiode sensitive at 1.3 mu m with picosecond time resolution. IEEE Journal of Quantum Electronics, 1992, 28, 2678-2681.	1.0	21
304	First demonstration of sub-nanosecond photon timing with a Germanium photodiode. Microelectronic Engineering, 1992, 19, 61-64.	1.1	1
305	Picosecond carrier dynamics and tunnelingâ€assisted recombination in photorefractive Î´â€doped superlattices. Applied Physics Letters, 1991, 58, 1375-1377.	1.5	2
306	Why the effective temperature of the hot electron tail approaches the lattice temperature. Applied Physics Letters, 1991, 59, 1623-1625.	1.5	17

#	Article	IF	Citations
307	Trapping phenomena in avalanche photodiodes on nanosecond scale. IEEE Electron Device Letters, 1991, 12, 685-687.	2.2	208
308	New double constant‑fraction trigger circuit for locking on laser pulse trains up to 100 MHz. Review of Scientific Instruments, 1990, 61, 1004-1009.	0.6	2
309	Photoluminescence lifetime microscope spectrometer based on time‑correlated single‑photon counting with an avalanche diode detector. Review of Scientific Instruments, 1990, 61, 11-22.	0.6	51
310	Observation of avalanche propagation by multiplication assisted diffusion in p‑n junctions. Applied Physics Letters, 1990, 57, 489-491.	1.5	49
311	Investigation of carrier transport in graded gap superlattices by time correlated single photon counting. Applied Physics Letters, 1990, 57, 2449-2451.	1.5	2
312	No dead-space optical time-domain reflectometer. Journal of Lightwave Technology, 1990, 8, 1278-1283.	2.7	23
313	20‑ps timing resolution with single‑photon avalanche diodes. Review of Scientific Instruments, 1989, 60, 1104-1110.	0.6	131
314	High-accuracy picosecond characterization of gain-switched laser diodes. Optics Letters, 1989, 14, 1341.	1.7	12
315	Four‑hundred‑picosecond single‑photon timing with commercially available avalanche photodiodes. Review of Scientific Instruments, 1988, 59, 1115-1121.	0.6	35