Long Zhang

List of Publications by Year
in descending order

63	477	840585 11	839398 18
papers	citations	h-index	g-index

63	63	63	203
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A 400-V Half Bridge Gate Driver for Normally-Off GaN HEMTs With Effective Dv/Dt Control and High Dv/Dt Immunity. IEEE Transactions on Industrial Electronics, 2023, 70, 741-751.	5.2	9
2	Influence of Different Device Structures on the Degradation for Trench-Gate SiC MOSFETs: Taking Avalanche Stress as an Example. Materials, 2022, 15, 457.	1.3	1
3	Unclamped-Inductive-Switching Behaviors of p-GaN HEMTs at Cryogenic Temperature. IEEE Transactions on Power Electronics, 2022, 37, 11507-11510.	5.4	3
4	A Silicon-On-Insulator Lateral IGBT With Segmented Trenches for Improving Short-Circuit Withstanding Capability. IEEE Transactions on Electron Devices, 2022, 69, 4042-4045.	1.6	5
5	Investigations on Unclamped-Inductive-Switching Behaviors of p-GaN HEMTs at Cryogenic Temperature. , 2022, , .		0
6	A High-voltage Silicon-On-Insulator Lateral IGBT with Segmented Trenches for Improved Short circuit Ruggedness. , 2022, , .		0
7	Investigations on Electrical Parameters Degradations of p-GaN HEMTs Under Repetitive UIS Stresses. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2021, 9, 2227-2234.	3.7	9
8	Study and Implementation of 600-V High-Voltage Gate Driver IC With the Common-Mode Dual-Interlock Technique for GaN Devices. IEEE Transactions on Industrial Electronics, 2021, 68, 1506-1514.	5.2	7
9	Investigation on the Degradation Mechanism for SiC Power MOSFETs Under Repetitive Switching Stress. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2021, 9, 2180-2189.	3.7	9
10	Simulation Study of A 1200V 4H-SiC Lateral MOSFET With Reduced Saturation Current. IEEE Electron Device Letters, 2021, 42, 1037-1040.	2.2	12
11	A 500V SOI-LIGBT With Multiple Deep-Oxide Trenches For Fast Turn-OFF. , 2021, , .		0
12	Low On-Resistance SOI-LDMOS With Mobility-Enhancing Auxiliary Cell. , 2021, , .		2
13	Investigation on the Single-event Burnout and Hardening of the 500V SOI Lateral-IGBT. , 2021, , .		2
14	Simulation Study of Novel Trench Gate U-Shaped Channel SOI Lateral IGBTs With Suppressed Gate Voltage Overshoot and Reduced di/dt. IEEE Transactions on Electron Devices, 2021, 68, 3930-3935.	1.6	2
15	Silicon-on-Insulator Lateral DMOS With Potential Modulation Plates and Multiple Deep-Oxide Trenches. IEEE Transactions on Electron Devices, 2021, 68, 5073-5077.	1.6	5
16	Reliability Concerns on LDMOS With Different Split-STI Layout Patterns. IEEE Transactions on Electron Devices, 2020, 67, 185-192.	1.6	6
17	Analysis of OFF-state dynamic avalanche instability in silicon-on-insulator lateral IGBTs at low temperature. Microelectronics Reliability, 2020, 107, 113600.	0.9	1
18	A self-adaptive pulse generator to realize extremely low power consumption and high reliability of high voltage gate driver IC. Analog Integrated Circuits and Signal Processing, 2020, 105, 13-20.	0.9	1

#	Article	IF	Citations
19	Experimental Investigation on the Electrical Properties of SOI-LIGBT Under Total-Ionizing-Dose Radiation. , 2020, , .		3
20	Highâ€temperature electrical performances and physicsâ€based analysis of pâ€GaN HEMT device. IET Power Electronics, 2020, 13, 420-425.	1.5	8
21	A Normally-off Copackaged SiC-JFET/GaN-HEMT Cascode Device for High-Voltage and High-Frequency Applications. IEEE Transactions on Power Electronics, 2020, 35, 9669-9679.	5.4	24
22	Super Field Plate Technique That Can Provide Charge Balance Effect for Lateral Power Devices Without Occupying Drift Region. IEEE Transactions on Electron Devices, 2020, 67, 2218-2222.	1.6	11
23	Integrated GaN MIS-HEMT with Multi-Channel Heterojunction SBD Structures. , 2019, , .		3
24	A 1200-V GaN/SiC cascode device with E-mode p-GaN gate HEMT and D-mode SiC junction field-effect transistor. Applied Physics Express, 2019, 12, 106505.	1.1	9
25	Impact of Depeltion in Substrate on Turn-off Characteristic of Superjunction SOI-LIGBT. , 2019, , .		2
26	Experimental Study on the Electrical Properties of Lateral IGBT Under the Mechanical Strain. , 2019, , .		1
27	Influence of Gate Connection Modes on Trade-offs in Trench Gate U-shaped Channel SOI-LIGBT. , 2019, , .		0
28	Mechanism and Novel Structure for di/dt Controllability in U-Shaped Channel Silicon-on-Insulator Lateral IGBTs. IEEE Electron Device Letters, 2019, 40, 1658-1661.	2.2	9
29	Hot-Carrier-Induced Degradation and Optimization for Lateral DMOS With Split-STI-Structure in the Drift Region. IEEE Transactions on Electron Devices, 2019, 66, 2869-2875.	1.6	3
30	Reliability concern of quasi-vertical GaN Schottky barrier diode under high temperature reverse bias stress. Superlattices and Microstructures, 2019, 130, 233-240.	1.4	4
31	Experimental Investigation on the Electrical Properties of Lateral IGBT Under Mechanical Strain. IEEE Electron Device Letters, 2019, 40, 937-940.	2.2	6
32	Anomalous output characteristics shrinkage in STI-LDMOS transistor after repetitive I-V scanning measurements. Superlattices and Microstructures, 2019, 128, 204-211.	1.4	0
33	Turn-Off Transient of Superjunction SOI Lateral IGBTs: Mechanism and Optimization Strategy. IEEE Transactions on Electron Devices, 2019, 66, 1409-1415.	1.6	11
34	A Novel Reverse Conducting SOI-LIGBT with Double Integrated NMOS for Enhanced Reverse Recovery. , 2019, , .		1
35	Low-Loss SOI-LIGBT With Assistant-Depletion Trench and Partial P-type Buried Layer. , 2019, , .		1
36	100 V Integrated Bootstrap Diode with Dynamic Field Limiting Rings for Solving Reverse Recovery Failure in GaN Gate Driver ICs. , 2019, , .		0

#	Article	IF	Citations
37	A 600V PiN diode with partial recessed anode and double-side Schottky engineering for fast reverse recovery. Superlattices and Microstructures, 2019, 128, 56-66.	1.4	0
38	500-V Silicon-On-Insulator Lateral IGBT With W-Shaped n-Typed Buffer and Composite p-Typed Collectors. IEEE Transactions on Electron Devices, 2019, 66, 1430-1434.	1.6	11
39	Influence of Emitter-side Deep-oxide Trenches on Dynamic Avalanche Capability of SOI Lateral IGBTs Used for Monolithic Power ICs. , 2018, , .		0
40	One cycle startâ€up time, high linearity relaxation oscillator with capacitor preâ€charge technique. Electronics Letters, 2018, 54, 1206-1208.	0.5	1
41	A high-speed SOI-LIGBT with electric potential modulation trench and low-doped buried layer. , 2018, , .		4
42	Optimization of <inline-formula> <tex-math notation="LaTeX">${V}_{ext{CE}}$ </tex-math> </inline-formula> Plateau for Deep-Oxide Trench SOI Lateral IGBT During Inductive Load Turn-OFF. IEEE Transactions on Electron Devices, 2018, 65, 3862-3868.	1.6	9
43	Novel Snapback-Free Reverse-Conducting SOI-LIGBT With Dual Embedded Diodes. IEEE Transactions on Electron Devices, 2017, 64, 1187-1192.	1.6	21
44	A U-Shaped Channel SOI-LIGBT With Dual Trenches. IEEE Transactions on Electron Devices, 2017, 64, 2587-2591.	1.6	16
45	Low-Loss SOI-LIGBT With Dual Deep-Oxide Trenches. IEEE Transactions on Electron Devices, 2017, 64, 3282-3286.	1.6	15
46	Comparison of short-circuit characteristics of trench gate and planar gate U-shaped channel SOI-LIGBTs. Solid-State Electronics, 2017, 135, 24-30.	0.8	6
47	A new high-voltage interconnection shielding method for SOI monolithic ICs. Solid-State Electronics, 2017, 133, 25-30.	0.8	7
48	Turn-off failure in multi-finger SOI-LIGBT used for single chip inverter ICs. Solid-State Electronics, 2017, 137, 29-37.	0.8	7
49	Fast recovery SOI PiN diode with multiple trenches. Superlattices and Microstructures, 2017, 111, 405-413.	1.4	4
50	Low-Loss SOI-LIGBT With Triple Deep-Oxide Trenches. IEEE Transactions on Electron Devices, 2017, 64, 3756-3761.	1.6	15
51	Analysis of clamped inductive turn-off failure of multi-finger lateral IGBT in SOI single chip inverter ICs. , 2017, , .		1
52	U-shaped channel SOI-LIGBT with dual trenches to improve the trade-off between saturation voltage and turn-off loss. , 2017, , .		6
53	Further Study of the U-Shaped Channel SOI-LIGBT With Enhanced Current Density for High-Voltage Monolithic ICs. IEEE Transactions on Electron Devices, 2016, 63, 1161-1167.	1.6	37
54	Electrical Characteristic Study of an SOI-LIGBT With Segmented Trenches in the Anode Region. IEEE Transactions on Electron Devices, 2016, 63, 2003-2008.	1.6	37

#	Article	IF	Citations
55	A novel high-voltage interconnection structure with dual trenches for 500V SOI-LIGBT. , 2016, , .		7
56	500 V SOI lateral pin diode with dual deepâ€oxide trenches for fast reverse recovery and suppressed oscillation. Electronics Letters, 2016, 52, 71-73.	0.5	0
57	A Novel Silicon-on-Insulator Lateral Insulated-Gate Bipolar Transistor With Dual Trenches for Three-Phase Single Chip Inverter ICs. IEEE Electron Device Letters, 2015, 36, 693-695.	2.2	28
58	500 V dual gate deepâ€oxide trench SOIâ€LIGBT with improved shortâ€circuit immunity. Electronics Letters, 2015, 51, 78-80.	0.5	2
59	A high current density SOI-LIGBT with Segmented Trenches in the Anode region for suppressing negative differential resistance regime. , 2015, , .		23
60	High voltage thick SOI-LIGBT with high current density and latch-up immunity. , 2015, , .		24
61	TC-LIGBTs on the Thin SoI Layer for the High Voltage Monolithic ICs With High Current Density and Latch-Up Immunity. IEEE Transactions on Electron Devices, 2014, 61, 3814-3820.	1.6	11
62	On state output characteristics and transconductance analysis of high voltage (600V) SJ-VDMOS. , 2012, , .		2
63	Electrical Characteristic Investigation on a Novel Double-Well Isolation Structure in 600-V-Class High-Voltage Integrated Circuits. IEEE Transactions on Electron Devices, 2012, 59, 3477-3481.	1.6	13