Davide De Caro

List of Publications by Year
in descending order

78 papers	1,908 citations	279798 23 h-index	276875 41 g-index
79 all docs	79 docs citations	79 times ranked	1016 citing authors

#	Article	IF	Citations
1	A Novel Module-Sign Low-Power Implementation for the DLMS Adaptive Filter With Low Steady-State Error. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 297-308.	5.4	6
2	Approximate Multipliers Using Static Segmentation: Error Analysis and Improvements. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2449-2462.	5.4	19
3	A Novel Low-Power High-Precision Implementation for Signâ€“Magnitude DLMS Adaptive Filters. Electronics (Switzerland), 2022, 11, 1007.	3.1	1
4	A novel low-power DLMS adaptive filter with sign-magnitude learning and approximated FIR section. , 2022, , .		0
5	A Binary Line Buffer Circuit Featuring Lossy Data Compression at Fixed Maximum Data Rate. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 121-134.	5.4	0
6	Low-Power Approximate Multiplier with Error Recovery using a New Approximate 4-2 Compressor. , 2020, , .		16
7	A 1.45 GHz All-Digital Spread Spectrum Clock Generator in 65nm CMOS for Synchronization-Free SoC Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3839-3852.	5.4	4
8	Comparison and Extension of Approximate 4-2 Compressors for Low-Power Approximate Multipliers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3021-3034.	5.4	141
9	Variable-Rounded LMS Filter for Low-Power Applications. Lecture Notes in Electrical Engineering, 2020, , 155-161.	0.4	1
10	Low-power Implementation of LMS Adaptive Filters Using Scalable Rounding. , 2020, , .		1
11	Low-Power Hardware Implementation of Least-Mean-Square Adaptive Filters Using Approximate Arithmetic. Circuits, Systems, and Signal Processing, 2019, 38, 5606-5622.	2.0	7
12	Design of Low-Power Approximate LMS Filters with Precision-Scalability. Lecture Notes in Electrical Engineering, 2019, , 237-243.	0.4	2
13	An FPGA-Oriented Algorithm for Real-Time Filtering of Poisson Noise in Video Streams, with Application to X-Ray Fluoroscopy. Circuits, Systems, and Signal Processing, 2019, 38, 3269-3294.	2.0	10
14	An FDD Wireless Diversity Receiver With Transmitter Leakage Cancellation in Transmit and Receive Bands. IEEE Journal of Solid-State Circuits, 2018, 53, 1945-1959.	5.4	18
15	Quality-Scalable Approximate LMS Filter. , 2018, , .		6
16	A Standard-Cell-Based All-Digital PWM Modulator With High Resolution and Spread- Spectrum Capability. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3885-3896.	5.4	18
17	On the Use of Approximate Multipliers in LMS Adaptive Filters. , 2018, , .		9
18	Approximate Multipliers Based on New Approximate Compressors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 4169-4182.	5.4	171

#	Article	IF	Citations
19	Stall-Aware Fixed-Point Implementation of LMS Filters. , 2018, , .		1
20	A SISO Register Circuit Tailored for Input Data with Low Transition Probability. IEEE Transactions on Computers, 2017, 66, 45-51.	3.4	1
21	Single Bit Filtering Circuit Implemented in a System for the Generation of Colored Noise. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1040-1050.	5.4	1
22	Minimizing Coefficients Wordlength for Piecewise-Polynomial Hardware Function Evaluation With Exact or Faithful Rounding. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1187-1200.	5.4	25
23	Single Flip-Flop Driving Circuit for Glitch-Free NAND-Based Digitally Controlled Delay-Lines. Circuits, Systems, and Signal Processing, 2017, 36, 1341-1360.	2.0	3
24	On the use of approximate adders in carry-save multiplier-accumulators. , 2017, , .		19
25	An Efficient Digital Background Control for Hybrid Transformer-Based Receivers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 3068-3080.	5.4	4
26	Variable Latency Speculative Parallel Prefix Adders for Unsigned and Signed Operands. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1200-1209.	5.4	47
27	Approximate adder with output correction for error tolerant applications and Gaussian distributed inputs. , 2016, , .		15
28	Hardware implementation of a spatio-temporal average filter for real-time denoising of fluoroscopic images. The Integration VLSI Journal, 2015, 49, 114-124.	2.1	11
29	A 3.3 GHz Spread-Spectrum Clock Generator Supporting Discontinuous Frequency Modulations in 28 nm CMOS. IEEE Journal of Solid-State Circuits, 2015, 50, 2074-2089.	5.4	15
30	Variable Latency Speculative Han-Carlson Adder. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1353-1361.	5.4	37
31	Variable latency speculative Han-Carlson adders topologies. , 2015, , .		6
32	High Speed Speculative Multipliers Based on Speculative Carry-Save Tree. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 3426-3435.	5.4	42
33	Analysis and comparison of Direct Digital Frequency Synthesizers implemented on FPGA. The Integration VLSI Journal, 2014, 47, 261-271.	2.1	13
34	Truncated squarer with minimum mean-square error. Microelectronics Journal, 2014, 45, 799-804.	2.0	10
35	Accurate Fixed-Point Logarithmic Converter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 526-530.	3.0	20
36	Fixed-Width Multipliers and Multipliers-Accumulators With Min-Max Approximation Error. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2375-2388.	5.4	44

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37	Glitch-Free NAND-Based Digitally Controlled Delay-Lines. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 55-66.	3.1	29
38	NORA based TDC in 90nm CMOS. Microelectronics Journal, 2013, 44, 489-495.	2.0	4
39	Optimal Discontinuous Frequency Modulation for Spread-Spectrum Clocking. IEEE Transactions on Electromagnetic Compatibility, 2013, 55, 891-900.	2.2	14
40	FPGA Implementation of Gaussian Mixture Model Algorithm for 47â€‰fps Segmentation of 1080p Video. Journal of Electrical and Computer Engineering, 2013, 2013, 1-8.	0.9	8
41	An Experimental Power-Lines Model for Digital ASICs Based on Transmission Lines. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 162-166.	3.1	0
42	A high-speed differential resistor ladder. Microelectronics Journal, 2012, 43, 433-438.	2.0	1
43	Efficient implementation of pseudochaotic piecewise linear maps with high digitization accuracies. International Journal of Circuit Theory and Applications, 2012, 40, 1-14.	2.0	8
44	Efficient Logarithmic Converters for Digital Signal Processing Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 667-671.	3.0	44
45	Direct Digital Frequency Synthesizer Using Nonuniform Piecewise-Linear Approximation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2409-2419.	5.4	25
46	Design of Fixed-Width Multipliers With Linear Compensation Function. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 947-960.	5.4	57
47	Elementary Functions Hardware Implementation Using Constrained Piecewise-Polynomial Approximations. IEEE Transactions on Computers, 2011, 60, 418-432.	3.4	47
48	A 41ps ASIC time-to-digital converter for physics experiments. Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2011, 659, 422-427.	1.6	10
49	A novel truncated squarer with linear compensation function. , 2010, , .		15
50	High-speed differential resistor ladder for A/D converters. , 2010, , .		1
51	Truncated Binary Multipliers With Variable Correction and Minimum Mean Square Error. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1312-1325.	5.4	96
52	A 1.27 GHz, All-Digital Spread Spectrum Clock Generator/Synthesizer in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 1048-1060.	5.4	128
53	High-Performance Special Function Unit for Programmable 3-D Graphics Processors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1968-1978.	5.4	40
54	Digital Synthesizer/Mixer With Hybrid CORDICâ€“Multiplier Architecture: Error Analysis and Optimization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 364-373.	5.4	17

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55	A 430 MHz, 280 mW Processor for the Conversion of Cartesian to Polar Coordinates in 0.25 $muhbox{m}$ CMOS. IEEE Journal of Solid-State Circuits, 2008, 43, 2503-2513.	5.4	18
56	A 2.5-GHz DDFS-PLL With 1.8-MHz Bandwidth in 0.35-mum CMOS. IEEE Journal of Solid-State Circuits, 2008, 43, 1403-1413.	5.4	21
57	A high performance floating-point special function unit using constrained piecewise quadratic approximation. , 2008, , .		5
58	Reducing Lookup-Table Size in Direct Digital Frequency Synthesizers Using Optimized Multipartite Table Method. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 2116-2127.	5.4	40
59	Constrained piecewise polinomial approximation for hardware implementation of elementary functions. , 2008, , .		2
60	Design of fixed-width multipliers with minimum mean square error. , 2007, , .		11
61	High Speed Galois Fields GF(2[?]) Multipliers. , 2007, , .		0
62	A 630 MHz, 76 mW Direct Digital Frequency Synthesizer Using Enhanced ROM Compression Technique. IEEE Journal of Solid-State Circuits, 2007, 42, 350-360.	5.4	43
63	A Novel Architecture for Galois Fields GF(2^m) Multipliers Based on Mastrovito Scheme. IEEE Transactions on Computers, 2007, 56, 1470-1483.	3.4	19
64	A 380 MHz Direct Digital Synthesizer/Mixer With Hybrid CORDIC Architecture in 0.25 $mu{hbox {m}}$ CMOS. IEEE Journal of Solid-State Circuits, 2007, 42, 151-160.	5.4	40
65	High-performance direct digital frequency synthesizers in 0.25 /spl mu/m CMOS using dual-slope approximation. IEEE Journal of Solid-State Circuits, 2005, 40, 2220-2227.	5.4	34
66	Dual-tree error compensation for high performance fixed-width multipliers. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2005, 52, 501-507.	2.2	62
67	High-performance direct digital frequency synthesizers using piecewise-polynomial approximation. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2005, 52, 324-337.	0.1	67
68	A novel high-speed sense-amplifier-based flip-flop. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 1266-1274.	3.1	71
69	Direct Digital Frequency Synthesizers With Polynomial Hyperfolding Technique. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2004, 51, 337-344.	2.2	48
70	Direct digital frequency synthesizers exploiting piecewise linear Chebyshev approximation. Microelectronics Journal, 2003, 34, 1099-1106.	2.0	5
71	Booth folding encoding for high performance squarer circuits. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2003, 50, 250-254.	2.2	38
72	Low-power flip-flops with reliable clock gating. Microelectronics Journal, 2001, 32, 21-28.	2.0	16

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73	Parallel squarer using Booth-folding technique. Electronics Letters, 2001, 37, 346.	1.0	23
74	Low power flip-flop with clock gating on master and slave latches. Electronics Letters, 2000, 36, 294.	1.0	36
75	Shuffled serial adder: an area-latency effective serial adder. , 0, , .		0
76	ROM-less direct digital frequency synthesizers exploiting polynomial approximation. , 0, , .		9
77	Direct digital frequency synthesis with dual-slope approach. , 0, , .		7
78	A high-speed sense-amplifier based flip-flop. , 0, , .		3