Carlos Marquez

List of Publications by Year
in descending order

38 papers	240 citations	1163117 8 h-index	1058476 14 g-index
40 all docs	40 docs citations	40 times ranked	287 citing authors

#	Article	IF	Citations
1	Performance of FDSOI double-gate dual-doped reconfigurable FETs. Solid-State Electronics, 2022, 194, 108336.	1.4	4
2	Hysteresis in As-Synthesized MoS2 Transistors: Origin and Sensing Perspectives. Micromachines, 2021, 12, 646.	2.9	3
3	Performance and reliability in back-gated CVD-grown MoS2 devices. Solid-State Electronics, 2021, 186, 108173.	1.4	2
4	Synthesis of graphene and other two-dimensional materials. , 2021, , 1-79.		4
5	Dual PN Source/Drain Reconfigurable FET for Fast and Low-Voltage Reprogrammable Logic. IEEE Access, 2020, 8, 132376-132381.	4.2	7
6	Investigating the transient response of Schottky barrier back-gated MoS₂ transistors. 2D Materials, 2020, 7, 025040.	4.4	13
7	CVD-grown back-gated MoS2 transistors. , 2020, , .		1
8	Systematic Characterization of Random Telegraph Noise and Its Dependence with Magnetic Fields in MOSFET Devices. , 2020, , 135-174.		2
9	Multi-Subband Ensemble Monte Carlo Simulator for Nanodevices in the End of the Roadmap. Lecture Notes in Computer Science, 2020, , 438-445.	1.3	2
10	Capacitor-less dynamic random access memory based on a IIIâ€“V transistor with a gate length of 14â€‰nm. Nature Electronics, 2019, 2, 412-419.	26.0	27
11	3-D TCAD Study of the Implications of Channel Width and Interface States on FD-SOI Z²-FETs. IEEE Transactions on Electron Devices, 2019, 66, 2513-2519.	3.0	8
12	Capacitorless memory devices using virtual junctions. , 2019, , .		0
13	Reliability Study of Thin-Oxide Zero-Ionization, Zero-Swing FET 1T-DRAM Memory Cell. IEEE Electron Device Letters, 2019, 40, 1084-1087.	3.9	10
14	Simulation Perspectives of Sub-1V Single-Supply Z²-FET 1T-DRAM Cells for Low-Power. IEEE Access, 2019, 7, 40279-40284.	4.2	8
15	Investigation of thin gate-stack Z2-FET devices as capacitor-less memory cells. Solid-State Electronics, 2019, 159, 12-18.	1.4	3
16	On the Low-Frequency Noise Characterization of Z²-FET Devices. IEEE Access, 2019, 7, 42551-42556.	4.2	4
17	Temperature and Gate Leakage Influence on the Z2-FET Memory Operation. , 2019, , .		1
18	Experimental Demonstration of Operational Z²-FET Memory Matrix. IEEE Electron Device Letters, 2018, 39, 660-663.	3.9	21

#	Article	IF	Citations
19	Gate Leakage Tunneling Impact on the InAs/GaSb Heterojunction Electronâ€“Hole Bilayer Tunneling Field-Effect Transistor. IEEE Transactions on Electron Devices, 2018, 65, 4679-4686.	3.0	8
20	Evaluation of thin-oxide Z2-FET DRAM cell. , 2018, , .		7
21	Experimental Characterization of the Random Telegraph Noise Signature in MOSFETs Under the Influence of Magnetic Fields. IEEE Electron Device Letters, 2018, 39, 1054-1057.	3.9	2
22	Towards InGaAs MSDRAM Capacitor-Less Cells. ECS Transactions, 2018, 85, 195-200.	0.5	3
23	InGaAs Capacitor-Less DRAM Cells TCAD Demonstration. IEEE Journal of the Electron Devices Society, 2018, 6, 884-892.	2.1	9
24	Insights on the Body Charging and Noise Generation by Impact Ionization in Fully Depleted SOI MOSFETs. IEEE Transactions on Electron Devices, 2017, 64, 5093-5098.	3.0	0
25	Systematic method for electrical characterization of random telegraph noise in MOSFETs. Solid-State Electronics, 2017, 128, 115-120.	1.4	5
26	Electrical characterization of Random Telegraph Noise in back-biased Ultrathin Silicon-On-Insulator MOSFETs. , 2016, , .		1
27	Electrical characterization and conductivity optimization of laser reduced graphene oxide on insulator using point-contact methods. RSC Advances, 2016, 6, 46231-46237.	3.6	16
28	Electrical characterization of Random Telegraph Noise in Fully-Depleted Silicon-On-Insulator MOSFETs under extended temperature range and back-bias operation. Solid-State Electronics, 2016, 117, 60-65.	1.4	17
29	Direct Characterization of Impact Ionization Current in Silicon-on-Insulator Body-Contacted MOSFETs. ECS Transactions, 2015, 66, 93-99.	0.5	2
30	Threshold voltage and on-current Variability related to interface traps spatial distribution. , 2015, , .		3
31	Determination of ad hoc deposited charge on bare SOI wafers. , 2015, , .		5
32	On the effective mobility extraction by point-contact techniques on silicon-on-insulator substrates. Journal of Applied Physics, 2015, 117, 035707.	2.5	8
33	Experimental developments of A2RAM memory cells on SOI and bulk substrates. Solid-State Electronics, 2015, 103, 7-14.	1.4	18
34	A2RAM: Low-power 1T-DRAM memory cells compatible with planar and 3D SOI substrates. , 2014, , .		0
35	In Situ Characterization of Bias Instability in Bare SOI Wafers by Pseudo-MOSFET Technique. IEEE Transactions on Device and Materials Reliability, 2014, 14, 878-883.	2.0	2
36	Tri-Dimensional A2-RAM Cell: Entering the Third Dimension. Engineering Materials, 2014, , 105-124.	0.6	0

#	Article	IF	Citations
37	Direct point-contact characterization of Bias instability on bare SOI wafers. , 2013, , .		1
38	Notice of Removal: Fabrication and validation of A2RAM memory cells on SOI and bulk substrates - Withdrawn. , 2013, , .		1