Gauthaman Murali

List of Publications by Year
in descending order

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		2258059	2550090
6	89	3	3
papers	citations	h-index	g-index

6	6	6	92
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Architecture, Chip, and Package Co-design Flow for 2.5D IC Design Enabling Heterogeneous IP Reuse. , 2019, , .		33
2	Architecture, Chip, and Package Codesign Flow for Interposer-Based 2.5-D Chiplet Integration Enabling Heterogeneous IP Reuse. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2424-2437.	3.1	32
3	Heterogeneous Mixed-Signal Monolithic 3-D In-Memory Computing Using Resistive RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 386-396.	3.1	18
4	Advances in Design and Test of Monolithic 3-D ICs. IEEE Design and Test, 2020, 37, 92-100.	1.2	6
5	Clock Delivery Network Design and Analysis for Interposer-Based 2.5-D Heterogeneous Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 605-616.	3.1	0
6	ParaMitE: Mitigating Parasitic CNFETs in the Presence of Unetched CNTs. , 2021, , .		0