Philip Brisk

List of Publications by Year
in descending order

136 papers	1,974 citations	471509 17 h-index	501196 28 g-index
140 all docs	140 docs citations	140 times ranked	1279 citing authors

#	Article	IF	Citations
1	BioScript. Communications of the ACM, 2021, 64, 97-104.	4.5	0
2	Time- and resource-constrained scheduling for digital microfluidic biochips. , 2021, , .		1
3	A pneumatic random-access memory for controlling soft robots. PLoS ONE, 2021, 16, e0254524.	2.5	17
4	Reducing Microfluidic Very Large-Scale Integration (mVLSI) Chip Area by Seam Carving. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2104-2116.	2.7	0
5	Rapid development and optimization of paper microfluidic designs using software automation. Analytica Chimica Acta, 2021, 1184, 338985.	5.4	1
6	Matrix Profile Index Approximation for Streaming Time Series. , 2021, , .		0
7	Dynamic Radial Placement and Routing in Paper Microfluidics. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, , 1-1.	2.7	1
8	ChemStor: Using Formal Methods To Guarantee Safe Storage and Disposal of Chemicals. Journal of Chemical Information and Modeling, 2020, 60, 3416-3422.	5.4	4
9	A performance-optimizing compiler for cyber-physical digital microfluidic biochips. , 2020, , .		8
10	Directed Placement for mVLSI Devices. ACM Journal on Emerging Technologies in Computing Systems, 2020, 16, 1-26.	2.3	3
11	Hardware-Assisted Cross-Generation Prediction of GPUs Under Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1133-1146.	2.7	1
12	TCAD EIC Message: February 2019. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 197-198.	2.7	0
13	Programmable Electrofluidics for Ionic Liquid Based Neuromorphic Platform. Micromachines, 2019, 10, 478.	2.9	3
14	Finding the optimal design of a passive microfluidic mixer. Lab on A Chip, 2019, 19, 3618-3627.	6.0	30
15	Using printer ink color to control the behavior of paper microfluidics. Lab on A Chip, 2019, 19, 2000-2008.	6.0	13
16	Chronoprints: Identifying Samples by Visualizing How They Change over Space and Time. ACS Central Science, 2019, 5, 589-598.	11.3	1
17	Matrix Profile XVIII: Time Series Mining in the Face of Fast Moving Streams using a Learned Approximate Matrix Profile. , 2019, , .		8
18	Approximate Adder Tree Synthesis for FPGAs. , 2019, , .		1

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19	Matrix Profile XIV. , 2019, , .		35
20	A compiler for cyber-physical digital microfluidic biochips. , 2018, , .		14
21	Exploiting a novel algorithm and GPUs to break the ten quadrillion pairwise comparisons barrier for time series motifs and joins. Knowledge and Information Systems, 2018, 54, 203-236.	3.2	24
22	Exploration of approximate multipliers design space using carry propagation free compressors. , 2018, , .		4
23	Scheduling and Fluid Routing for Flow-Based Microfluidic Laboratories-on-a-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 615-628.	2.7	16
24	Resource-Constrained Scheduling for Digital Microfluidic Biochips. ACM Journal on Emerging Technologies in Computing Systems, 2018, 14, 1-26.	2.3	8
25	Deterministic Parallel Routing for FPGAs Based on Galois Parallel Execution Model. , 2018, , .		7
26	A compiler for cyber-physical digital microfluidic biochips. , 2018, , .		0
27	HLSPredict. , 2018, , .		24
28	ParchMint: A Microfluidics Benchmark Suite. , 2018, , .		3
29	BioScript: programming safe chemistry on laboratories-on-a-chip. , 2018, 2, 1-31.		17
30	Stationary-Mixing Field-Programmable Pin-Constrained Digital Microfluidic Biochip. Microelectronics Journal, 2018, 77, 34-48.	2.0	2
31	Approximate quaternary addition with the fast carry chains of FPGAs. , 2018, , .		10
32	Accelerating Simulation of Particle Trajectories in Microfluidic Devices by Constructing a Cloud Database. , 2018, , .		2
33	Predictive Modeling for CPU, GPU, and FPGA Performance and Power Consumption: A Survey. , 2018, , .		26
34	Performance Improvements and Congestion Reduction for Routing-Based Synthesis for Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 41-54.	2.7	20
35	PCB Escape Routing and Layer Minimization for Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 69-82.	2.7	14
36	Arbitrary Precision and Complexity Tradeoffs for Gate-Level Information Flow Tracking. , 2017, , .		4

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37	Design Automation for Paper Microfluidics with Passive Flow Substrates. , 2017, , .		3
38	GPU Performance Estimation using Software Rasterization and Machine Learning. Transactions on Embedded Computing Systems, 2017, 16, 1-21.	2.9	7
39	HALWPE. , 2017, , .		9
40	The case for semi-automated design of microfluidic very large scale integration (mVLSI) chips. , 2017, , .		3
41	An Out-of-Order Load-Store Queue for Spatial Computing. , 2017, , .		2
42	MOPSA: A microfluidics-optimized particle simulation algorithm. Biomicrofluidics, 2017, 11, 034121.	2.4	6
43	CAL: Exploring cost, accuracy, and latency in approximate and speculative adder design. , 2017, , .		3
44	Diagonal Component Expansion for Flow-Layer Placement of Flow-Based Microfluidic Biochips. Transactions on Embedded Computing Systems, 2017, 16, 1-18.	2.9	17
45	An Out-of-Order Load-Store Queue for Spatial Computing. Transactions on Embedded Computing Systems, 2017, 16, 1-19.	2.9	119
46	From C to elastic circuits. , 2017, , .		8
47	Instantaneous simulation of fluids and particles in complex microfluidic devices. PLoS ONE, 2017, 12, e0189429.	2.5	17
48	Reducing Microfluidic Very Large Scale Integration (mVLSI) Chip Area by Seam Carving. , 2017, , .		2
49	Matrix Profile II: Exploiting a Novel Algorithm and GPUs to Break the One Hundred Million Barrier for Time Series Motifs and Joins. , 2016, , .		126
50	Random design of microfluidics. Lab on A Chip, 2016, 16, 4212-4219.	6.0	41
51	Automatic Application of Power Analysis Countermeasures. IEEE Transactions on Computers, 2015, 64, 329-341.	3.4	31
52	Rapid online fault recovery for cyber-physical digital microfluidic biochips. , 2015, , .		27
53	Simulation of feedback-driven PCR assays on a 2D electrowetting array using a domain-specific high-level biological programming language. Microelectronic Engineering, 2015, 148, 110-116.	2.4	7
54	Graph-Based Approaches to Placement of Processing Element Networks on FPGAs for Physical Model Simulation. ACM Transactions on Reconfigurable Technology and Systems, 2015, 7, 1-22.	2.5	1

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55	Fast and Memory-Efficient Routing Algorithms for Field Programmable Gate Arrays With Sparse Intracluster Routing Crossbars. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1928-1941.	2.7	9
56	An open-source compiler and PCB synthesis tool for digital microfluidic biochips. The Integration VLSI Journal, 2015, 51, 169-193.	2.1	50
57	Flow-Layer Physical Design for Microchips Based on Monolithic Membrane Valves. IEEE Design and Test, 2015, 32, 51-59.	1.2	10
58	Exploring speed and energy tradeoffs in droplet transport for digital microfluidic biochips. , 2014, , .		5
59	A Low-Cost Field-Programmable Pin-Constrained Digital Microfluidic Biochip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1657-1670.	2.7	20
60	Accelerating the dynamic time warping distance measure using logarithmetic arithmetic. , 2014, , .		1
61	Multi-terminal PCB escape routing for digital microfluidic biochips using negotiated congestion. , 2014, , .		4
62	Performance and cost analysis of NoC-inspired virtual topologies for digital microfluidic biochips. , 2014, , .		1
63	Simulated annealing-based placement for microfluidic large scale integration (mLSI) chips. , 2014, , .		19
64	Interpreting Assays with Control Flow on Digital Microfluidic Biochips. ACM Journal on Emerging Technologies in Computing Systems, 2014, 10, 1-30.	2.3	17
65	Recent developments in microfluidic large scale integration. Current Opinion in Biotechnology, 2014, 25, 60-68.	6.6	88
66	Fast Online Synthesis of Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 356-369.	2.7	52
67	Virtual Ways: Low-Cost Coherence for Instruction Set Extensions with Architecturally Visible Storage. Transactions on Architecture and Code Optimization, 2014, 11, 1-26.	2.0	0
68	Parallel FPGA Routing based on the Operator Formulation. , 2014, , .		32
69	Way Stealing: A Unified Data Cache and Architecturally Visible Storage for Instruction Set Extensions. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 62-75.	3.1	5
70	A Just-in-Time Customizable processor. , 2013, , .		12
71	Introduction to the special issue on application-specific processors. Transactions on Embedded Computing Systems, 2013, 13, 1-3.	2.9	0
72	A field-programmable pin-constrained digital microfluidic biochip. , 2013, , .		39

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73	Automatic synthesis of microfluidic large scale integration chips from a domain-specific language. , 2013, , .		7
74	Instruction set extensions for Dynamic Time Warping. , 2013, , .		6
75	Design and verification tools for continuous fluid flow-based microfluidic devices. , 2013, , .		11
76	Shared memory heterogeneous computation on PCIe-supported platforms. , 2013, , .		7
77	A high-performance online assay interpreter for digital microfluidic biochips. , 2012, , .		12
78	Path scheduling on digital microfluidic biochips. , 2012, , .		60
79	Reducing the cost of floating-point mantissa alignment and normalization in FPGAs. , 2012, , .		5
80	Fast online synthesis of generally programmable digital microfluidic biochips. , 2012, , .		51
81	SSI Properties Revisited. Transactions on Embedded Computing Systems, 2012, 11S, 1-23.	2.9	7
82	Force-Directed List Scheduling for Digital Microfluidic Biochips. , 2012, , .		10
83	Routing algorithms for FPGAS with sparse intra-cluster routing crossbars. , 2012, , .		3
84	A digital microfluidic biochip synthesis framework. , 2012, , .		1
85	Force-Directed List Scheduling for Digital Microfluidic Biochips. , 2012, , .		1
86	Counting stream registers: An efficient and effective snoop filter architecture. , 2012, , .		2
87	A digital microfluidic biochip synthesis framework. , 2012, , .		16
88	Architecture and design automation for application-specific processors. , 2011, , .		0
89	Graph-coloring and treescan register allocation using repairing. , 2011, , .		14
90	Compressor tree synthesis on commercial high-performance FPGAs. ACM Transactions on Reconfigurable Technology and Systems, 2011, 4, 1-19.	2.5	35

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91	A high-level synthesis flow for custom instruction set extensions for application-specific processors. , 2010, , .		14
92	Synthesis of Floating-Point Addition Clusters on FPGAs Using Carry-Save Arithmetic. , 2010, , .		4
93	Improving FPGA Performance for Carry-Save Arithmetic. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 578-590.	3.1	24
94	Fast, Nearly Optimal ISE Identification With I/O Serialization Through Maximal Clique Enumeration. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 341-354.	2.7	16
95	An Optimal Linear-Time Algorithm for Interprocedural Register Allocation in High Level Synthesis Using SSA Form. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1096-1109.	2.7	1
96	Architectural support for the orchestration of fine-grained multiprocessing for portable streaming applications. , 2009, , .		1
97	Iterative layering. , 2009, , .		3
98	On the complexity of the Port Assignment Problem for Binary Commutative Operators in high-level synthesis. , 2009, , .		4
99	Way Stealing. , 2009, , .		19
100	An approximation algorithm for scheduling on heterogeneous reconfigurable resources. Transactions on Embedded Computing Systems, 2009, 9, 1-20.	2.9	5
101	An FPGA Logic Cell and Carry Chain Configurable as a 6:2 or 7:2 Compressor. ACM Transactions on Reconfigurable Technology and Systems, 2009, 2, 1-42.	2.5	3
102	Field Programmable Compressor Trees. ACM Transactions on Reconfigurable Technology and Systems, 2009, 2, 1-36.	2.5	9
103	Optimistic chordal coloring: a coalescing heuristic forÂSSAÂform programs. Design Automation for Embedded Systems, 2009, 13, 115-137.	1.0	3
104	FPGA Implementation of a Single-Precision Floating-Point Multiply-Accumulator with Single-Cycle Accumulation. , 2009, , .		11
105	A flexible DSP block to enhance FPGA arithmetic performance. , 2009, , .		4
106	Hybrid LZA: A near optimal implementation of the Leading Zero Anticipator. , 2009, , .		3
107	Exploiting fast carry-chains of FPGAs for designing compressor trees. , 2009, , .		33
108	Challenges in Automatic Optimization of Arithmetic Circuits. , 2009, , .		8

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109	Using 3D integration technology to realize multi-context FPGAs. , 2009, , .		2
110	Arithmetic optimization for custom instruction set synthesis. , 2009, , .		1
111	Introducing control-flow inclusion to support pipelining in custom instruction set extensions. , 2009, , .		9
112	MPSoC Design Using Application-Specific Architecturally Visible Communication. Lecture Notes in Computer Science, 2009, , 183-197.	1.3	3
113	A Design Flow and Evaluation Framework for DPA-Resistant Instruction Set Extensions. Lecture Notes in Computer Science, 2009, , 205-219.	1.3	41
114	Reconfigurable Embedded Medical Systems. , 2009, , 228-240.		0
115	Efficient synthesis of compressor trees on FPGAs. , 2008, , .		34
116	Data-Flow Transformations to Maximize the Use of Carry-Save Representation in Arithmetic Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1761-1774.	2.7	30
117	Scheduling of dataflow models within the Reconfigurable Video Coding framework. , 2008, , .		12
118	Variable Latency Speculative Addition: A New Paradigm for Arithmetic Circuit Design. , 2008, , .		70
119	A novel FPGA logic block for improved arithmetic performance. , 2008, , .		10
120	Fast, quasi-optimal, and pipelined instruction-set extensions. , 2008, , .		7
121	Architectural improvements for field programmable counter arrays. , 2008, , .		6
122	Design space exploration for field programmable compressor trees. , 2008, , .		2
123	Improving synthesis of compressor trees on FPGAs via integer linear programming. , 2008, , .		18
124	Improving Synthesis of Compressor Trees on FPGAs via Integer Linear Programming. , 2008, , .		13
125	Speculative DMA for architecturally visible storage in instruction set extensions. , 2008, , .		15
126	Interference graphs for procedures in static single information form are interval graphs. , 2007, , .		6

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127	Enhancing FPGA performance for arithmetic circuits. Proceedings - Design Automation Conference, 2007, , .	0.0	13
128	Optimal polynomial-time interprocedural register allocation for high-level synthesis and ASIP design. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	4
129	Rethinking custom ISE identification. , 2007, , .		40
130	An optimistic and conservative register assignment heuristic for chordal graphs. , 2007, , .		3
131	Delay aware, reconfigurable security for embedded systems. , 2007, , .		4
132	Datapath Synthesis. , 2007, , 233-255.		0
133	A dictionary construction technique for code compression systems with echo instructions. ACM SIGPLAN Notices, 2005, 40, 105-114.	0.2	2
134	Adaptive and fault tolerant medical vest for life-critical medical monitoring. , 2005, , .		36
135	Instruction Selection for Compilers That Target Architectures with Echo Instructions. Lecture Notes in Computer Science, 2004, , 229-243.	1.3	3
136	Instruction generation and regularity extraction for reconfigurable processors. , 2002, , .		51