VÃ-ctor M. Brea

List of Publications by Year
in descending order

61 papers	656 citations	623188 14 h-index	642321 23 g-index
61 all docs	61 docs citations	61 times ranked	553 citing authors

#	Article	IF	Citations
1	Tracking more than 100 arbitrary objects at 25 FPS through deep learning. Pattern Recognition, 2022, 121, 108205.	5.1	12
2	An 11 mA Capacitor-Less LDO With 3.08 nA Quiescent Current and SSF-Based Adaptive Biasing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 844-848.	2.2	8
3	Short-term anchor linking and long-term self-guided attention for video object detection. Image and Vision Computing, 2021, 110, 104179.	2.7	8
4	Real-Time Multiple Object Visual Tracking for Embedded GPU Systems. IEEE Internet of Things Journal, 2021, 8, 9177-9188.	5.5	16
5	STDnet-ST: Spatio-temporal ConvNet for small object detection. Pattern Recognition, 2021, 116, 107929.	5.1	31
6	All-hardware SIFT implementation for real-time VGA images feature extraction. Journal of Real-Time Image Processing, 2020, 17, 371-382.	2.2	6
7	On-Chip Solar Energy Harvester and PMU With Cold Start-Up and Regulated Output Voltage for Biomedical Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1103-1114.	3.5	21
8	Special issue on smart cameras for real-time image and video processing. Journal of Real-Time Image Processing, 2020, 17, 1755-1756.	2.2	2
9	STDnet: Exploiting high resolution feature maps for small object detection. Engineering Applications of Artificial Intelligence, 2020, 91, 103615.	4.3	48
10	Real-time visual detection and tracking system for traffic monitoring. Engineering Applications of Artificial Intelligence, 2019, 85, 410-420.	4.3	49
11	Ultralow power voltage reference circuit for implantable devices in standard CMOS technology. International Journal of Circuit Theory and Applications, 2019, 47, 991-1005.	1.3	4
12	Deep Learning-Based Multiple Object Visual Tracking on Embedded System for IoT and Mobile Edge Computing Applications. IEEE Internet of Things Journal, 2019, 6, 5423-5431.	5.5	70
13	Micro-Energy Harvesting System Including a PMU and a Solar Cell on the Same Substrate With Cold Startup From 2.38 nW and Input Power Range up to 10 muW Using Continuous MPPT. IEEE Transactions on Power Electronics, 2019, 34, 5105-5116.	5.4	25
14	Inâ€pixel analog memories for a pixelâ€based background subtraction algorithm on CMOS vision sensors. International Journal of Circuit Theory and Applications, 2018, 46, 1631-1647.	1.3	6
15	Special issue on advances on smart camera architectures for real-time image processing. Journal of Real-Time Image Processing, 2018, 14, 635-636.	2.2	4
16	Pulsed timeâ€ofâ€flight pixel with onâ€chip 20Âklux background light suppression in standard CMOS technology. International Journal of Circuit Theory and Applications, 2018, 46, 987-1005.	1.3	0
17	Wireless Sensor Network With Perpetual Motes for Terrestrial Snail Activity Monitoring. IEEE Sensors Journal, 2017, 17, 5008-5015.	2.4	21
18	Low-Power CMOS Vision Sensor for Gaussian Pyramid Extraction. IEEE Journal of Solid-State Circuits, 2017, 52, 483-495.	3.5	23

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19	Dynamic Model of Switched-Capacitor DCâ€“DC Converters in the Slow-Switching Limit Including Charge Reusing. IEEE Transactions on Power Electronics, 2017, 32, 5293-5311.	5.4	14
20	Dynamic joint model of capacitive charge pumps and onâ€chip photovoltaic cells for CMOS microâ€energy harvesting. International Journal of Circuit Theory and Applications, 2016, 44, 1874-1894.	1.3	6
21	PRECISION: A Reconfigurable SIMD/MIMD Coprocessor for Computer Vision Systems-on-Chip. IEEE Transactions on Computers, 2016, 65, 2548-2561.	2.4	5
22	Image Feature Extraction Acceleration. Studies in Computational Intelligence, 2016, , 109-132.	0.7	1
23	Four-transistor pinned photodiodes in standard CMOS technologies for time-of-flight sensors. Semiconductor Science and Technology, 2015, 30, 045002.	1.0	2
24	Distance Measurement Error in Time-of-Flight Sensors Due to Shot Noise. Sensors, 2015, 15, 4624-4642.	2.1	28
25	A 26.5 nJ/px 2.64 Mpx/s CMOS vision sensor for Gaussian pyramid extraction. , 2014, , .		5
26	Split and shift methodology on cellular processor arrays: area saving versus time penalty. International Journal of Circuit Theory and Applications, 2014, 42, 258-295.	1.3	0
27	The dickson charge pump as voltage booster for light energy harvesting on CMOS vision chips. , 2014, , .		3
28	Custom design of pinned photodiodes in standard CMOS technologies for time-of-flight sensors. , 2014, , .		1
29	Gaussian pyramid extraction with a CMOS vision sensor. , 2014, , .		1
30	Dark current in standard CMOS pinned photodiodes for Time-of-Flight sensors. , 2014, , .		3
31	Form factor improvement of smart-pixels for vision sensors through 3-D vertically-integrated technologies. , 2014, , .		1
32	A hierarchical vision processing architecture oriented to 3D integration of smart camera chips. Journal of Systems Architecture, 2013, 59, 908-919.	2.5	9
33	A 176×120 pixel CMOS vision chip for Gaussian filtering with massivelly Parallel CDS and A/D-conversion. , 2013, , .		4
34	Voltage boosters for on-chip solar cells on focal-plane processors. , 2013, , .		0
35	CMOS-3D Smart Imager Architectures for Feature Detection. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2012, 2, 723-736.	2.7	19
36	In-pixel generation of gaussian pyramid images by block reusing in 3D-CMOS. , 2012, , .		0

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37	SIMD/MIMD Dynamically-Reconfigurable Architecture for High-Performance Embedded Vision Systems. , 2012, , .		12
38	Performance analysis of massively parallel embedded hardware architectures for retinal image processing. Eurasip Journal on Image and Video Processing, 2011, 2011, .	1.7	8
39	A 3D chip architecture for optical sensing and concurrent processing. Proceedings of SPIE, 2010, , .	0.8	6
40	FPGA-accelerated retinal vessel-tree extraction. , 2009, , .		14
41	Handsheet for full-custom circuit design. , 2009, , .		0
42	A digital cellular-based system for retinal vessel-tree extraction. , 2009, , .		1
43	Effect of Mismatch on the Reliability of ON/OFF-Programmable CNNs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 2259-2269.	3.5	1
44	An efficient FPGA implementation of a DT-CNN for small image gray-scale pre-processing. , 2009, , .		2
45	SIMD array on FPGA for B/W image processing. , 2008, , .		6
46	Template-oriented hardware design based on shape analysis of 2D CNN operators in CNN template libraries and applications. , 2008, , .		3
47	Verification of Split&Shift techniques for CNN hardware reduction. , 2007, , .		3
48	Relating Cellular Non-linear Networks to Threshold Logic and Single Instruction Multiple Data computing models. , 2007, , .		0
49	CNN Implementation of Spin Filters for Electronic Speckle Pattern Interferometry Applications. , 2007, , .		1
50	Area and Time Efficient Cellular Non-linear Networks. , 2007, , .		3
51	On the Reduction of the Number of Coefficient Circuits in a DTCNN Cell. , 2006, , .		7
52	A binary-based on-chip CNN solution for pixel-level snakes. International Journal of Circuit Theory and Applications, 2006, 34, 383-407.	1.3	12
53	Design of the Processing Core of a Mixed-Signal CMOS DTCNN Chip for Pixel-Level Snakes. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 997-1013.	0.1	22
54	Cellular neural networks and active contours: a tool for image segmentation. Image and Vision Computing, 2003, 21, 189-204.	2.7	45

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55	Robustness oriented design tool for multilayer DTCNN applications. International Journal of Circuit Theory and Applications, 2002, 30, 195-210.	1.3	5
56	Discrete-time CNN for image segmentation by active contours. Pattern Recognition Letters, 1998, 19, 721-734.	2.6	33
57	Robustness improvement in binary cellular non-linear network architectures. , 0, , .		3
58	Implementation oriented theory design issues on the DTCNN template generation. , 0, , .		0
59	An analogic CNN-algorithm of pixel level snakes for tracking and surveillance tasks. , 0, , .		3
60	A One-Quadrant Discrete-Time Cellular Neural Network CMOS Chip for Pixel-Level Snakes. , 0, , .		5
61	A One-Quadrant Discrete-Time Cellular Neural Network Architecture for Pixel-Level Snakes: B/W Processing. , 0, , .		5