Yan aibin

List of Publications by Year
in descending order

55	1,186	331670 21	414414 32
papers	citations	h-index	g-index

55	55	55	487
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Novel Quadruple-Node-Upset-Tolerant Latch Designs With Optimized Overhead for Reliable Computing in Harsh Radiation Environments. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 404-413.	4.6	49
2	Cost-Effective and Highly Reliable Circuit-Components Design for Safety-Critical Applications. IEEE Transactions on Aerospace and Electronic Systems, 2022, 58, 517-529.	4.7	20
3	Evaluation and Test of Production Defects in Hardened Latches. IEICE Transactions on Information and Systems, 2022, E105.D, 996-1009.	0.7	1
4	A double-node-upset completely tolerant CMOS latch design with extremely low cost for high-performance applications. The Integration VLSI Journal, 2022, 86, 22-29.	2.1	4
5	Quadruple and Sextuple Cross-Coupled SRAM Cell Designs With Optimized Overhead for Reliable Applications. IEEE Transactions on Device and Materials Reliability, 2022, 22, 282-295.	2.0	34
6	SCLCRL: Shuttling C-elements based Low-Cost and Robust Latch Design Protected against Triple Node Upsets in Harsh Radiation Environments. , 2022, , .		3
7	Designs of Level-Sensitive T Flip-Flops and Polar Encoders Based on Two XOR/XNOR Gates. Electronics (Switzerland), 2022, 11, 1658.	3.1	5
8	Two 0.8 V, Highly Reliable RHBD 10T and 12T SRAM Cells for Aerospace Applications. , 2022, , .		0
9	Sextuple Cross-Coupled-DICE Based Double-Node-Upset Recoverable and Low-Delay Flip-Flop for Aerospace Applications. , 2022, , .		0
10	A Highly Robust, Low Delay and DNU-Recovery Latch Design for Nanoscale CMOS Technology. , 2022, , .		1
11	A Highly Reliable and Low Power RHBD Flip-Flop Cell for Aerospace Applications. , 2022, , .		1
12	Machine learning classification algorithm for VLSI test cost reduction. The Integration VLSI Journal, 2022, 87, 40-48.	2.1	5
13	Broadcast-TDMA: A Cost-Effective Fault-Tolerance Method for TSV Lifetime Reliability Enhancement. IEEE Design and Test, 2022, 39, 34-42.	1.2	3
14	A Novel TDMA-Based Fault Tolerance Technique for the TSVs in 3D-ICs Using Honeycomb Topology. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 724-734.	4.6	39
15	Novel Low Cost, Double-and-Triple-Node-Upset-Tolerant Latch Designs for Nano-scale CMOS. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 520-533.	4.6	68
16	A Cost-Effective TSV Repair Architecture for Clustered Faults in 3-D IC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1952-1956.	2.7	29
17	TPDICE and Sim Based 4-Node-Upset Completely Hardened Latch Design for Highly Robust Computing in Harsh Radiation. , 2021, , .		7
18	Dual-modular-redundancy and dual-level error-interception based triple-node-upset tolerant latch designs for safety-critical applications. Microelectronics Journal, 2021, 111, 105034.	2.0	8

#	Article	IF	Citations
19	A 4NU-Recoverable and HIS-Insensitive Latch Design for Highly Robust Computing in Harsh Radiation Environments. , 2021, , .		5
20	A Reliable and Low-Cost Flip-Flop Hardened against Double-Node-Upsets. , 2021, , .		1
21	A Sextuple Cross-Coupled Dual-Interlocked-Storage-Cell based Multiple-Node-Upset Self-Recoverable Latch. , 2021, , .		3
22	Design of a Triple-Node-Upset Self-Recoverable Latch for Aerospace Applications in Harsh Radiation Environments. IEEE Transactions on Aerospace and Electronic Systems, 2020, 56, 1163-1171.	4.7	52
23	LCHR-TSV: Novel Low Cost and Highly Repairable Honeycomb-Based TSV Redundancy Architecture for Clustered Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2938-2951.	2.7	55
24	Non-Intrusive Online Distributed Pulse Shrinking-Based Interconnect Testing in 2.5D IC. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2657-2661.	3.0	40
25	A Novel Low-Cost TMR-Without-Voter Based HIS-Insensitive and MNU-Tolerant Latch Design for Aerospace Applications. IEEE Transactions on Aerospace and Electronic Systems, 2020, 56, 2666-2676.	4.7	24
26	Quadruple Cross-Coupled Dual-Interlocked-Storage-Cells-Based Multiple-Node-Upset-Tolerant Latch Designs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 879-890.	5.4	32
27	HITTSFL: Design of a Cost-Effective HIS-Insensitive TNU-Tolerant and SET-Filterable Latch for Safety-Critical Applications. , 2020, , .		3
28	Novel Speed-and-Power-Optimized SRAM Cell Designs With Enhanced Self-Recoverability From Single- and Double-Node Upsets. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4684-4695.	5.4	50
29	Pattern Reorder for Test Cost Reduction Through Improved SVMRANK Algorithm. IEEE Access, 2020, 8, 147965-147972.	4.2	10
30	Dual-Interlocked-Storage-Cell-Based Double-Node-Upset Self-Recoverable Flip-Flop Design for Safety-Critical Applications. , 2020, , .		4
31	Architecture of Cobweb-Based Redundant TSV for Clustered Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1736-1739.	3.1	132
32	Information Assurance Through Redundant Design: A Novel TNU Error-Resilient Latch for Harsh Radiation Environment. IEEE Transactions on Computers, 2020, 69, 789-799.	3.4	66
33	A Sextuple Cross-Coupled SRAM Cell Protected against Double-Node Upsets. , 2020, , .		3
34	A Double-Node-Upset Self-Recoverable Latch Design for High Performance and Low Power Application. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 287-291.	3.0	29
35	A Novel Triple-Node-Upset-Tolerant CMOS Latch Design using Single-Node-Upset-Resilient Cells. , 2019, , .		13
36	Novel Application of Deep Learning for Adaptive Testing Based on Long Short-Term Memory. , 2019, , .		6

#	Article	IF	Citations
37	Single-Event Double-Upset Self-Recoverable and Single-Event Transient Pulse Filterable Latch Design for Low Power Applications. , 2019, , .		10
38	Novel Radiation Hardened Latch Design with Cost-Effectiveness for Safety-Critical Terrestrial Applications. , 2019, , .		1
39	Novel Quadruple Cross-Coupled Memory Cell Designs With Protection Against Single Event Upsets and Double-Node Upsets. IEEE Access, 2019, 7, 176188-176196.	4.2	20
40	Design of a Sextuple Cross-Coupled SRAM Cell with Optimized Access Operations for Highly Reliable Terrestrial Applications. , 2019, , .		4
41	Novel Double-Node-Upset-Tolerant Memory Cell Designs Through Radiation-Hardening-by-Design and Layout. IEEE Transactions on Reliability, 2019, 68, 354-363.	4.6	37
42	Novel low cost and DNU online self-recoverable RHBD latch design for nanoscale CMOS. , 2018, , .		2
43	T2FA: Transparent Two-Factor Authentication. IEEE Access, 2018, 6, 32677-32686.	4.2	38
44	Single event double-upset fully immune and transient pulse filterable latch design for nanoscale CMOS. Microelectronics Journal, 2017, 61, 43-50.	2.0	26
45	Double-Node-Upset-Resilient Latch Design for Nanoscale CMOS Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1978-1982.	3.1	86
46	HLDTL: High-performance, low-cost, and double node upset tolerant latch design. , 2017, , .		5
47	A single event transient detector in SRAM-based FPGAs. IEICE Electronics Express, 2017, 14, 20170210-20170210.	0.8	5
48	Highly Robust Double Node Upset Resilient Hardened Latch Design. IEICE Transactions on Electronics, 2017, E100.C, 496-503.	0.6	6
49	A Region-Based Through-Silicon via Repair Method for Clustered Faults. IEICE Transactions on Electronics, 2017, E100.C, 1108-1117.	0.6	13
50	A transient pulse dually filterable and online self-recoverable latch. IEICE Electronics Express, 2017, 14, 20160911-20160911.	0.8	6
51	An SEU resilient, SET filterable and cost effective latch in presence of PVT variations. Microelectronics Reliability, 2016, 63, 239-250.	1.7	32
52	Highâ€performance, lowâ€cost, and highly reliable radiation hardened latch design. Electronics Letters, 2016, 52, 139-141.	1.0	24
53	A Self-Recoverable, Frequency-Aware and Cost-Effective Robust Latch Design for Nanoscale CMOS Technology. IEICE Transactions on Electronics, 2015, E98.C, 1171-1178.	0.6	41
54	Design of a Radiation Hardened Latch for Low-Power Circuits. , 2014, , .		21

#	Article	IF	Citations
55	Design of Radiation Hardened Latch and Flip-Flop with Cost-Effectiveness for Low-Orbit Aerospace Applications. Journal of Electronic Testing: Theory and Applications (JETTA), 0, , 1.	1.2	4