Liang Shi

List of Publications by Year
in descending order

80 papers	1,076 citations	623574 14 h-index	610775 24 g-index
80 all docs	80 docs citations	80 times ranked	799 citing authors

#	Article	IF	Citations
1	Optimizing Data Placement for Hybrid SRAM+Racetrack Memory SPM in Embedded Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 847-859.	1.9	3
2	Tail Latency Optimization for LDPC-Based High-Density and Low-Cost Flash Memory Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 544-557.	1.9	2
3	DWR: Differential Wearing for Read Performance Optimization on High-Density NAND Flash Memory. , 2022, , .		2
4	Read latency variation aware performance optimization on high-density NAND flash based storage systems. CCF Transactions on High Performance Computing, 2022, 4, 265-280.	1.1	1
5	Read-Ahead Efficiency on Mobile Devices: Observation, Characterization, and Optimization. IEEE Transactions on Computers, 2021, 70, 99-110.	2.4	2
6	iTRIM: I/O-Aware TRIM for Improving User Experience on Mobile Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1782-1795.	1.9	2
7	High Thought Control Ability, High Resilience: The Effect of Temporal Cortex and Insula Connectivity. Neuroscience, 2021, 472, 60-67.	1.1	7
8	MobileSwap: Cross-Device Memory Swapping for Mobile Devices. , 2021, , .		3
9	Understanding and Optimizing Hybrid SSD with High-Density and Low-Cost Flash Memory. , 2021, , .		4
10	Dynamic File Cache Optimization for Hybrid SSDs with High-Density and Low-Cost Flash Memory. , 2021, , .		2
11	Brain Entropy is Associated with Divergent Thinking. Cerebral Cortex, 2020, 30, 708-717.	1.6	30
12	Process Variation Aware Read Performance Improvement for LDPC-Based nand Flash Memory. IEEE Transactions on Reliability, 2020, 69, 310-321.	3.5	11
13	Maximizing I/O Throughput and Minimizing Performance Variation via Reinforcement Learning Based I/O Merging for SSDs. IEEE Transactions on Computers, 2020, 69, 72-86.	2.4	11
14	Aging Capacitor Supported Cache Management Scheme for Solid-State Drives. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2230-2239.	1.9	4
15	SEAL: User Experience-Aware Two-Level Swap for Mobile Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4102-4114.	1.9	9
16	A Zero-Energy Consumption Scheme for System Suspend to Limited NVM. , 2020, , .		0
17	Boosting the Performance of SSDs via Fully Exploiting the Plane Level Parallelism. IEEE Transactions on Parallel and Distributed Systems, 2020, 31, 2185-2200.	4.0	12
18	Exploiting Asymmetric Errors for LDPC Decoding Optimization on 3D NAND Flash Memory. IEEE Transactions on Computers, 2020, 69, 475-488.	2.4	24

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19	Effects of the Openness to Experience Polygenic Score on Cortical Thickness and Functional Connectivity. Frontiers in Neuroscience, 2020, 14, 607912.	1.4	1
20	Architectural Exploration on Racetrack Memories. , 2020, , .		1
21	An Empirical Study of Hybrid SSD with Optane and QLC Flash. , 2020, , .		4
22	Minimizing Retention Induced Refresh Through Exploiting Process Variation of Flash Memory. IEEE Transactions on Computers, 2019, 68, 83-98.	2.4	20
23	Constructing Large, Durable and Fast SSD System via Reprogramming 3D TLC Flash Memory. , 2019, , .		23
24	Brain Functional Basis of Subjective Well-being During Negative Facial Emotion Processing Task-Based fMRI. Neuroscience, 2019, 423, 177-191.	1.1	13
25	Fair Down to the Device: A GC-Aware Fair Scheduler for SSD. , 2019, , .		2
26	Optimizing Tail Latency of LDPC based Flash Memory Storage Systems Via Smart Refresh. , 2019, , .		4
27	1+1>2: variation-aware lifetime enhancement for embedded 3D NAND flash systems. , 2019, , .		5
28	Parallel all the time: Plane Level Parallelism Exploration for High Performance SSDs. , 2019, , .		10
29	File Fragmentation in Mobile Devices: Measurement, Evaluation, and Treatment. IEEE Transactions on Mobile Computing, 2019, 18, 2062-2076.	3.9	9
30	Brain connection pattern under interoceptive attention state predict interoceptive intensity and subjective anxiety feeling. Human Brain Mapping, 2019, 40, 1760-1773.	1.9	16
31	Recover from the adversity: functional connectivity basis of psychological resilience. Neuropsychologia, 2019, 122, 20-27.	0.7	50
32	Openness to experience and psychophysiological interaction patterns during divergent thinking. Brain Imaging and Behavior, 2019, 13, 1580-1589.	1.1	13
33	Potential Trigger Detection for Hardware Trojans. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1384-1395.	1.9	13
34	Energy, latency, and lifetime improvements in MLC NVM with enhanced WOM code. , 2018, , .		7
35	Large-scale brain network connectivity underlying creativity in resting-state and task fMRI: Cooperation between default network and frontal-parietal network. Biological Psychology, 2018, 135, 102-111.	1.1	74
36	ApproxFTL: On the Performance and Lifetime Improvement of 3-D NAND Flash-Based SSDs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1957-1970.	1.9	24

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37	Exploiting Parallelism for Access Conflict Minimization in Flash-Based Solid State Drives. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 168-181.	1.9	32
38	An I/O Scheduling Strategy for Embedded Flash Storage Devices With Mapping Cache. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 756-769.	1.9	8
39	Selective Compression Scheme for Read Performance Improvement on Flash Devices. , 2018, , .		3
40	F2FS Aware Mapping Cache Design on Solid State Drives. , 2018, , .		5
41	Work-in-Progress: Revisiting Wear Leveling Design on Compression Applied 3D NAND Flash Memory. , 2018, , .		3
42	Exploiting Chip Idleness for Minimizing Garbage Collectionâ€"Induced Chip Access Conflict on SSDs. ACM Transactions on Design Automation of Electronic Systems, 2018, 23, 1-29.	1.9	14
43	Brain networks of happiness: dynamic functional connectivity among the default, cognitive and salience networks relates to subjective well-being. Social Cognitive and Affective Neuroscience, 2018, 13, 851-862.	1.5	52
44	An Efficient Cache Management Scheme for Capacitor Equipped Solid State Drives. , 2018, , .		2
45	Access Characteristic Guided Read and Write Regulation on Flash Based Storage Systems. IEEE Transactions on Computers, 2018, 67, 1663-1676.	2.4	12
46	Improving LDPC performance via asymmetric sensing level placement on flash memory. , 2017, , .		33
47	Improving read performance via selective V_{pass} reduction on high density 3D NAND flash memory. , 2017, , .		2
48	Asymmetric Error Rates of Cell States Exploration for Performance Improvement on Flash Memory Based Storage Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1340-1352.	1.9	5
49	Reducing LDPC Soft Sensing Latency by Lightweight Data Refresh for Flash Read Performance Improvement. , 2017, , .		26
50	Exploiting Process Variation for Read Performance Improvement on LDPC Based Flash Memory Storage Systems. , 2017, , .		5
51	Towards trustworthy storage using SSDs with proprietary FTL. Microprocessors and Microsystems, 2017, 55, 82-90.	1.8	3
52	An empirical study of F2FS on mobile devices. , 2017, , .		7
53	Minimizing cell-to-cell interference by exploiting differential bit impact characteristics of scaled MLC NAND flash memories. , 2016, , .		3
54	Dynamic merging/splitting for better responsiveness in mobile devices. , 2016, , .		6

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55	PUMA: From Simultaneous to Parallel for Shared Memory System in Multi-core. Journal of Signal Processing Systems, 2016, 84, 139-150.	1.4	1
56	Peak-to-average pumping efficiency improvement for charge pump in Phase Change Memories. , 2016, , .		3
57	Write reconstruction for write throughput improvement on MLC PCM based main memory. Journal of Systems Architecture, 2016, 71, 62-72.	2.5	3
58	A New Design of In-Memory File System Based on File Virtual Address Framework. IEEE Transactions on Computers, 2016, 65, 2959-2972.	2.4	43
59	Retention Trimming for Lifetime Improvement of Flash Memory Storage Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 58-71.	1.9	32
60	Exploiting Process Variation for Write Performance Improvement on NAND Flash Memory Storage Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 334-337.	2.1	33
61	Exploiting Process Variation for Retention Induced Refresh Minimization on Flash Memory. , 2016, , .		18
62	Towards Trustable Storage using SSDs with Proprietary FTL. , 2015, , .		3
63	Designing an efficient persistent in-memory file system. , 2015, , .		12
64	Compiler-Assisted Refresh Minimization for Volatile STT-RAM Cache. IEEE Transactions on Computers, 2015, 64, 2169-2181.	2.4	20
65	Wear Relief for High-Density Phase Change Memory Through Cell Morphing Considering Process Variation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 227-237.	1.9	14
66	Improving MLC PCM write throughput by write reconstruction. , 2015, , .		4
67	Maximizing IO Performance Via Conflict Reduction for Flash Memory Storage Systems. , 2015, , .		12
68	Exploit asymmetric error rates of cell states to improve the performance of flash memory storage systems. , 2014, , .		10
69	Combine thread with memory scheduling for maximizing performance in multi-core systems. , 2014, , .		2
70	High-level synthesis for run-time hardware Trojan detection and recovery. , 2014, , .		12
71	Retention trimming for wear reduction of flash memory storage systems. , 2014, , .		7
72	PUMA: Pseudo unified memory architecture for single-ISA heterogeneous multi-core systems. , 2014, , .		0

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73	Exploiting parallelism in I/O scheduling for access conflict minimization in flash-based solid state drives. , 2014, , .		60
74	Error Model Guided Joint Performance and Endurance Optimization for Flash Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 343-355.	1.9	14
75	A Unified Write Buffer Cache Management Scheme for Flash Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2779-2792.	2.1	10
76	Compiler-Assisted STT-RAM-Based Hybrid Cache for Energy Efficient Embedded Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1829-1840.	2.1	32
77	Relaxed wear leveling approach for non-volatile memories. , 2013, , .		3
78	Accurate age counter for wear leveling on non-volatile based main memory. Design Automation for Embedded Systems, 2013, 17, 543-564.	0.7	4
79	ExLRU. , 2011, , .		37
80	Write activity reduction on flash main memory via smart victim cache. , 2010, , .		48