Mahmut T Kandemir

List of Publications by Year
in descending order

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68	780	840585 11	713332 21
papers	citations	h-index	g-index

68	68	68	682
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Predicting Proteinâ€“Ligand Docking Structure with Graph Neural Network. Journal of Chemical Information and Modeling, 2022, 62, 2923-2932.	2.5	23
2	Guiding Conventional Proteinâ€“Ligand Docking Software with Convolutional Neural Networks. Journal of Chemical Information and Modeling, 2020, 60, 4594-4602.	2.5	15
3	DÃ©jÃ View: Spatio-Temporal Compute Reuse forâ€˜ Energy-Efficient 360Â° VR Video Streaming. , 2020, , .		11
4	Affine Modeling of Program Traces. IEEE Transactions on Computers, 2019, 68, 294-300.	2.4	4
5	CaSym: Cache Aware Symbolic Execution for Side Channel Detection and Mitigation. , 2019, , .		34
6	A Scale-Out Enterprise Storage Architecture. , 2017, , .		2
7	ZombieNAND: Resurrecting Dead NAND Flash for Improved SSD Longevity. , 2014, , .		8
8	Quantifying and Optimizing the Impact of Victim Cache Line Selection in Manycore Systems. , 2014, , .		0
9	Will They Blend?: Exploring Big Data Computation Atop Traditional HPC NAS Storage. , 2014, , .		8
10	Improved cache utilization and preconditioner efficiency through use of a space-filling curve mesh element- and vertex-reordering technique. Engineering With Computers, 2014, 30, 535-547.	3.5	6
11	Compiler-Directed Energy Reduction Using Dynamic Voltage Scaling and Voltage Islands for Embedded Systems. IEEE Transactions on Computers, 2013, 62, 268-278.	2.4	23
12	Traffic steering between a low-latency unswitched TL ring and a high-throughput switched on-chip interconnect. , 2013, , .		2
13	Examining Thread Vulnerability analysis using fault-injection. , 2013, , .		2
14	Reshaping cache misses to improve row-buffer locality in multicore systems. , 2013, , .		10
15	AUTOMATIC PARALLEL CODE GENERATION FOR NUFFT DATA TRANSLATION ON MULTICORES. Journal of Circuits, Systems and Computers, 2012, 21, 1240004.	1.0	1
16	Performance-reliability tradeoff analysis for multithreaded applications. , 2012, , .		0
17	IOPin: Runtime Profiling of Parallel I/O in HPC Systems. , 2012, , .		15
18	MROrchestrator: A Fine-Grained Resource Orchestration Framework for MapReduce Clusters. , 2012, , .		30

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19	Locality-Aware Dynamic Mapping for Multithreaded Applications. , 2012, , .		0
20	Physically Addressed Queueing (PAQ): Improving parallelism in Solid State Disks. , 2012, , .		9
21	An Evolutionary Path to Object Storage Access. , 2012, , .		6
22	Exploring performance-power tradeoffs in providing reliability for NoC-based MPSoCs. , 2011, , .		2
23	Improving energy efficiency of multi-threaded applications using heterogeneous CMOS-TFET multicores. , 2011, , .		16
24	Quantifying Thread Vulnerability for Multicore Architectures. , 2011, , .		2
25	Exploring heterogeneous NoC design space. , 2011, , .		7
26	Optimizing Data Layouts for Parallel Computation on Multicores. , 2011, , .		19
27	Neighborhood-aware data locality optimization for NoC-based multicores. , 2011, , .		4
28	Particle simulation on the Cell BE architecture. Cluster Computing, 2011, 14, 419-432.	3.5	0
29	Feedback control based cache reliability enhancement for emerging multicores. , 2011, , .		4
30	Total Power Optimization for Combinational Logic Using Genetic Algorithms. Journal of Signal Processing Systems, 2010, 58, 145-160.	1.4	5
31	A special-purpose compiler for look-up table and code generation for function evaluation. , 2010, , .		1
32	Analyzing the soft error resilience of linear solvers on multicore multiprocessors. , 2010, , .		21
33	Intra-application cache partitioning. , 2010, , .		14
34	Feedback control for providing QoS in NoC based multicores. , 2010, , .		8
35	CPM in CMPs: Coordinated Power Management in Chip-Multiprocessors. , 2010, , .		52
36	T-NUCA - a novel approach to non-uniform access latency cache architectures for 3D CMPs. , 2010, , .		1

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37	Adaptive prefetching for shared cache based chip multiprocessors. , 2009, , .		2
38	A hardware-software codesign strategy for Loop intensive applications. , 2009, , .		5
39	Process-Variation-Aware Adaptive Cache Architecture and Management. IEEE Transactions on Computers, 2009, 58, 865-877.	2.4	20
40	An Automated Framework for Accelerating Numerical Algorithms on Reconfigurable Platforms Using Algorithmic/Architectural Optimization. IEEE Transactions on Computers, 2009, 58, 1654-1667.	2.4	4
41	Using Data Compression for Increasing Memory System Utilization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 901-914.	1.9	8
42	Designing a 3-D FPGA: Switch Box Architecture and Thermal Issues. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 882-893.	2.1	40
43	Compiler-Directed Code Restructuring for Improving Performance of MPSoCs. IEEE Transactions on Parallel and Distributed Systems, 2008, 19, 1201-1214.	4.0	7
44	Towards energy efficient scaling of scientific codes. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	5
45	A helper thread based EDP reduction scheme for adapting application execution in CMPs. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	27
46	Managing power, performance and reliability trade-offs. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	0
47	Improving I/O performance through compiler-directed code restructuring and adaptive prefetching. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	0
48	Evaluating the role of scratchpad memories in chip multiprocessors for sparse matrix computations. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	3
49	Runtime system support for software-guided disk power management. , 2007, , .		0
50	Memory Bank Aware Dynamic Loop Scheduling. , 2007, , .		2
51	Improving MPI Independent Write Performance Using A Two-Stage Write-Behind Buffering Method. , 2007, , .		6
52	Reducing Data TLB Power via Compiler-Directed Address Generation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 312-324.	1.9	11
53	Solving the Register Allocation Problem for Embedded Systems Using a Hybrid Evolutionary Algorithm. IEEE Transactions on Evolutionary Computation, 2007, 11, 620-634.	7.5	17
54	Reducing Energy Consumption of On-Chip Networks Through a Hybrid Compiler-Runtime Approach. Parallel Architecture and Compilation Techniques (PACT), Proceedings of the International Conference on, 2007, , .	0.0	1

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55	On the Detection of Clones in Sensor Networks Using Random Key Predistribution. IEEE Transactions on Systems, Man and Cybernetics, Part C: Applications and Reviews, 2007, 37, 1246-1258.	3.3	110
56	Data locality enhancement for CMPs. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	3
57	Enhancing Locality in Two-Dimensional Space through Integrated Computation and Data Mappings. , 2007, , .		1
58	Integrated Data Reorganization and Disk Mapping for Reducing Disk Energy Consumption. , 2007, , .		3
59	Compiler-Directed Energy Optimization for Parallel Disk Based Systems. IEEE Transactions on Parallel and Distributed Systems, 2007, 18, 1241-1257.	4.0	9
60	Reducing energy consumption of parallel sparse matrix applications through integrated link/CPU voltage scaling. Journal of Supercomputing, 2007, 41, 179-213.	2.4	16
61	Energy-Aware Code Replication for Improving Reliability in Embedded Chip Multiprocessors. , 2006, , .		3
62	Discretionary Caching for I/O on Clusters. Cluster Computing, 2006, 9, 29-44.	3.5	11
63	The Sleep Deprivation Attack in Sensor Networks: Analysis and Methods of Defense. International Journal of Distributed Sensor Networks, 2006, 2, 267-287.	1.3	85
64	Compiler Support for Voltage Islands. , 2006, , .		3
65	Switch Box Architectures for Three-Dimensional FPGAs. , 2006, , .		4
66	Optimizing Leakage Energy Consumption in Cache Bitlines. Design Automation for Embedded Systems, 2004, 9, 5-18.	0.7	2
67	Energy-performance trade-offs for spatial access methods on memory-resident data. VLDB Journal, 2002, 11, 179-197.	2.7	5
68	Increasing Data TLB Resilience to Transient Errors. , 0, , .		2