Rutu Parekh

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/7139704/publications.pdf

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15	84	1937685 4	1474206 9
papers	citations	h-index	g-index

20	20	20	50
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Single-electron transistor: review in perspective of theory, modelling, design and fabrication. Microsystem Technologies, 2021, 27, 1863-1875.	2.0	14
2	Design and implementation of single electron transistor based 8X8 bit signed multipliers. Materials Today: Proceedings, 2021, 43, 3904-3910.	1.8	0
3	Design strategy and simulation of single-gate SET for novel SETMOS hybridization. Journal of Computational Electronics, 2021, 20, 218-229.	2.5	0
4	Design of prominent Time-to-Digital Converter using single electron transistor operating at room temperature. , 2020, , .		0
5	Design of prominent SETâ€based high performance computing system. IET Circuits, Devices and Systems, 2020, 14, 159-167.	1.4	4
6	A New Tool for Simulation of Single Electron Transistor based Microprocessor Using Vector File. Nanoscience and Nanotechnology - Asia, 2020, 10, 493-500.	0.7	0
7	Strategy for Designing Single Electron Transistors. Communications in Computer and Information Science, 2020, , 44-57.	0.5	1
8	A Novel Slice-Based High-Performance ALU Design Using Prospective Single Electron Transistor. IETE Journal of Research, 2019, , 1-10.	2.6	4
9	A Vector File Generation Program for Simulating Single Electron Transistor based Computing System. , 2018, , .		4
10	Noise Removing Filters and Its Implementation on FPGA. Lecture Notes in Electrical Engineering, 2018, , 481-489.	0.4	3
11	Modeling and Simulation of 1/f Noise During Threshold Switching for Phase Change Memory. Lecture Notes in Electrical Engineering, 2018, , 77-83.	0.4	1
12	Performance Analysis of Current-Mode Interconnect System in Presence of Process, Voltage, and Temperature Variations. Lecture Notes in Electrical Engineering, 2018, , 543-551.	0.4	1
13	Design and Optimization of Single Electron Transistor Based 4-Bit Arithmetic and Logic Unit at Room Temperature Operation. , 2017, , .		1
14	SET logic driving capability and its enhancement in 3-D integrated SETâ€“CMOS circuit. Microelectronics Journal, 2014, 45, 1087-1092.	2.0	16
15	Simulation and Design Methodology for Hybrid SET-CMOS Integrated Logic at 22-nm Room-Temperature Operation. IEEE Transactions on Electron Devices, 2012, 59, 918-923.	3.0	28