Xuewen Zeng

List of Publications by Year in descending order

Source: https://exaly.com/author-pdf/7136205/publications.pdf

Version: 2024-02-01

24 papers	888 citations	1478505 6 h-index	1281871 11 g-index
24 all docs	24 docs citations	24 times ranked	628 citing authors

#	Article	IF	Citations
1	End-to-end encrypted traffic classification with one-dimensional convolution neural networks. , 2017, , .		434
2	HAST-IDS: Learning Hierarchical Spatial-Temporal Features Using Deep Neural Networks to Improve Intrusion Detection. IEEE Access, 2018, 6, 1792-1806.	4.2	388
3	Dynamic Inertia Weight Binary Bat Algorithm with Neighborhood Search. Computational Intelligence and Neuroscience, 2017, 2017, 1-15.	1.7	17
4	A Packet-Length-Adjustable Attention Model Based on Bytes Embedding Using Flow-WGAN for Smart Cybersecurity. IEEE Access, 2019, 7, 82913-82926.	4.2	12
5	High-Performance Implementation of Dynamically Configurable Load Balancing Engine on FPGA. IEEE Communications Magazine, 2020, 58, 62-67.	6.1	11
6	A Blockchain-Based Decentralized Public Key Infrastructure for Information-Centric Networks. Information (Switzerland), 2022, 13, 264.	2.9	8
7	A Fast, Smart Packet Classification Algorithm Based on Decomposition. Journal of Control Science and Engineering, 2020, 2020, 1-11.	1.0	7
8	High Throughput Implementation of SMS4 on FPGA. IEEE Access, 2019, 7, 88836-88844.	4.2	4
9	A distributed and virtualized infrastructure for networked multimedia services. , 2013, , .		1
10	Online Resource Monitoring Model in Cloud TV. , 2013, , .		1
11	A storage approach for OpenFlow switch based on Protocol Oblivious Forwarding. , 2016, , .		1
12	An Adaptive Throughput-First Packet Scheduling Algorithm for DPDK-Based Packet Processing Systems. Future Internet, 2021, 13, 78.	3.8	1
13	Accelerating the SM3 hash algorithm with CPUâ€FPGA Coâ€Ðesigned architecture. IET Computers and Digital Techniques, 2021, 15, 427.	1.2	1
14	A Multifunctional Full-Packet Capture and Network Measurement System Supporting Nanosecond Timestamp and Real-Time Analysis. IEEE Transactions on Instrumentation and Measurement, 2021, 70, 1-12.	4.7	1
15	Fast Montgomery Modular Multiplication and Squaring on Embedded Processors. IEICE Transactions on Communications, 2017, E100.B, 680-690.	0.7	1
16	Time-Shifting Proxy Resource Scheduling Strategy Based on Predictable User Behaviors. , 2008, , .		0
17	Goodput guaranteed buffer management strategy for streaming data with packet dependencies. , 2016, , .		0
18	Optimal Buffer Management Strategy for Minimizing Delivery Latency of Streaming Data with Packet Dependencies. IEICE Transactions on Communications, 2016, E99.B, 1501-1510.	0.7	0

#	Article	IF	Citations
19	SSL transmission delay optimization in multi-core processor based on network path delay prediction. , 2017, , .		0
20	PREPARE-Playback RatE and Priority Adaptive BitRate Selection. IEEE Access, 2019, 7, 135352-135362.	4.2	0
21	Research on Multicore Key-Value Storage System for Domain Name Storage. Applied Sciences (Switzerland), 2021, 11, 7425.	2.5	0
22	A Register Access Control Scheme for SNR System to Counter CPA Attack Based on Malicious User Blacklist. Future Internet, 2021, 13, 262.	3.8	0
23	A High Performance Multi Core Network Processing System. , 2011, , 439-443.		0
24	Reputation-Based Sharding Consensus Model in Information-Centric Networking. Electronics (Switzerland), 2022, 11, 830.	3.1	0