Chung-Kuan Cheng

List of Publications by Year in Descending Order

98 papers	761 citations	16 h-index	21 g-index
141 ext. papers	1,089 ext. citations	2.2 avg, IF	3.96 L-index

#	Paper	IF	Citations
98	Machine Learning Prediction for Design and System Technology Co-Optimization Sensitivity Analysis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2022**, 1-14	2.6	
97	Complementary-FET (CFET) Standard Cell Synthesis Framework for Design and System Technology Co-Optimization Using SMT. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 1178-1191	2.6	8
96	Many-Tier Vertical Gate-All-Around Nanowire FET Standard Cell Synthesis for Advanced Technology Nodes. *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, **2021**, 7, 52-60	2.4	2
95	Multirow Complementary-FET (CFET) Standard Cell Synthesis Framework Using Satisfiability Modulo Theories (SMTs). *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, **2021**, 7, 43-51	2.4	2
94	SAT-Based On-Track Bus Routing. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 735-747	2.5	0
93	PROBE2.0: A Systematic Framework for Routability Assessment from Technology to Design in Advanced Nodes. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	2
92	SMT-based Contention-Free Task Mapping and Scheduling on SMART NoC. *IEEE Embedded Systems Letters*, **2021**, 1-1	1	1
91	Arnoldi Algorithms with Structured Orthogonalization. *SIAM Journal on Numerical Analysis*, **2021**, 59, 370-400	2.4	
90	Resting-state magnetoencephalography source magnitude imaging with deep-learning neural network for classification of symptomatic combat-related mild traumatic brain injury. *Human Brain Mapping*, **2021**, 42, 1987-2004	5.9	2
89	Design and System Technology Co-Optimization Sensitivity Prediction for VLSI Technology Development using Machine Learning **2021**,		1
88	Standard-Cell Scaling Framework with Guaranteed Pin-Accessibility **2020**,		2
87	SP&R: Simultaneous Placement and Routing framework for standard cell synthesis in sub-7nm **2020** ,		5
86	Stability and Convergency Exploration of Matrix Exponential Integration on Power Delivery Network Transient Simulation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 2735-2748	2.5	3
85	Grid-Based Framework for Routability Analysis and Diagnosis With Conditional Design Rules. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 5097-5110	2.5	6
84	A routability-driven complimentary-FET (CFET) standard cell synthesis framework using SMT **2020**,		5
83	SP&R: SMT-Based Simultaneous Place-and-Route for Standard Cell Synthesis of Advanced Nodes. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 1-1	2.5	2
82	Marked Increases in Resting-State MEG Gamma-Band Activity in Combat-Related Mild Traumatic Brain Injury. *Cerebral Cortex*, **2020**, 30, 283-295	5.1	10

81	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 1717-1730	2.5	21
80	ROAD **2019**,		7
79	MEG Working Memory N-Back Task Reveals Functional Deficits in Combat-Related Mild Traumatic Brain Injury. *Cerebral Cortex*, **2019**, 29, 1953-1968	5.1	9
78	Transient circuit simulation for differential algebraic systems using matrix exponential **2018**,		2
77	Fast and precise routability analysis with conditional design rules **2018**,		11
76	Exploring the exponential integrators with Krylov subspace algorithms for nonlinear circuit simulation **2017**,		3
75	ePlace-3D **2016**,		11
74	A fast time-domain EM□CAD coupled simulation framework via matrix exponential with stiffness reduction. *International Journal of Circuit Theory and Applications*, **2016**, 44, 833-850	2	
73	An Efficient Transient Electro-Thermal Simulation Framework for Power Integrated Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 832-843	2.5	9
72	Simulation Algorithms With Exponential Integration for Time-Domain Analysis of Large-Scale Power Delivery Networks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1681-1694	2.5	11
71	From Circuit Theory, Simulation to SPICEDiego: A Matrix Exponential Approach for Time-Domain Analysis of Large-Scale Circuits. *IEEE Circuits and Systems Magazine*, **2016**, 16, 16-34	3.2	10
70	ePlace. *ACM Transactions on Design Automation of Electronic Systems*, **2015**, 20, 1-34	1.5	27
69	ePlace-MS: Electrostatics-Based Placement for Mixed-Size Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 685-698	2.5	28
68	Dynamic analysis of power delivery network with nonlinear components using matrix exponential method **2015**,		2
67	Ratio of the Worst Case Noise and the Impedance of Power Distribution Network. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2014**, 4, 1325-1334	1.7	
66	Worst Case Noise Prediction With Nonzero Current Transition Times for Power Grid Planning. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 607-620	2.6	
65	Energy Efficiency Optimization Through Codesign of the Transmitter and Receiver in High-Speed On-Chip Interconnects. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 938-942	2.6	10
64	Developing an EEG-based on-line closed-loop lapse detection and mitigation system. *Frontiers in Neuroscience*, **2014**, 8, 321	5.1	28

63	ePlace **2014**,		17
62	Performance-driven placement for design of rotation and right arithmetic shifters in monolithic 3D ICs **2013**,		4
61	Modeling and Analysis of Power Distribution Networks in 3-D ICs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 354-366	2.6	8
60	Novel Differential-Mode Equalizer With Broadband Common-Mode Filtering for Gb/s Differential-Signal Transmission. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2013**, 3, 1578-1587	1.7	12
59	Power grid simulation using matrix exponential method with rational Krylov subspaces **2013**,		8
58	A Realistic Early-Stage Power Grid Verification Algorithm Based on Hierarchical Constraints. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 109-120	2.5	12
57	A Practical Regularization Technique for Modified Nodal Analysis in Large-Scale Time-Domain Circuit Simulation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1031-1040	2.5	16
56	Time-Domain Analysis of Large-Scale Circuits by Matrix Exponential Method With Adaptive Control. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1180-1193	2.5	20
55	Cell-phone based Drowsiness Monitoring and Management system **2012**,		6
54	Eye prediction of digital driver with power distribution network noise **2012**,		5
53	Ultra-low power on-chip differential interconnects using high-resolution comparator **2012**,		1
52	Analysis and Optimization of Low-Power Passive Equalizers for CPU Memory Links. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2011**, 1, 1406-1420	1.7	4
51	On-Chip Interconnect Analysis of Performance and Energy Metrics Under Different Design Goals. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 520-524	2.6	7
50	Prediction and Comparison of High-Performance On-Chip Global Interconnection. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 1154-1166	2.6	11
49	Bus Matrix Synthesis Based on Steiner Graphs for Power Efficient System-on-Chip Communications. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 167-179	2.5	1
48	A block-diagonal structured model reduction scheme for power grid networks **2011**,		4
47	A fast and stable explicit integration method by matrix exponential operator for large scale circuit simulation **2011**,		3
46	High-speed and low-power on-chip global link using continuous-time linear equalizer **2010**,		5

45	Efficient Power Network Analysis with Modeling of Inductive Effects. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2010**, E93-A, 1196-1203	0.4	1
44	Parallel transistor level circuit simulation using domain decomposition methods **2009**,		12
43	Enhancing Learning Effectiveness in Digital Design Courses Through the Use of Programmable Logic Boards. *IEEE Transactions on Education*, **2009**, 52, 151-156	2.1	24
42	Efficient power network analysis with complete inductive modeling **2009**,		1
41	Parallel transistor level full-chip circuit simulation **2009**,		5
40	Symmetrical buffer placement in clock trees for minimal skew immune to global on-chip variations **2009**,		1
39	Accurate Eye Diagram Prediction Based on Step Response and Its Aication to Low-Power Equalizer Design. *IEICE Transactions on Electronics*, **2009**, E92-C, 444-452	0.4	11
38	Efficient Partial Reluctance Extraction for Large-Scale Regular Power Grid Structures. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2009**, E92-A, 1476-1484	0.4	1
37	Digital design and programmable logic boards: Do students actually learn more? **2008**,		5
36	A novel fixed-outline floorplanner with zero deadspace for hierarchical design **2008**,		3
35	Efficient frequency-dependent reluctance extraction for large-scale Power/Ground grid **2008**,		1
34	Efficient and accurate eye diagram prediction for high speed signaling **2008**,		21
33	Exploring Cardioneural Signals from Noninvasive ECG Measurement **2007**,		1
32	Optimum Prefix Adders in a Comprehensive Area, Timing and Power Design Space **2007**,		12
31	Efficient timing analysis with known false paths using biclique covering. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 959-969	2.5	
30	Two-stage newton□aphson method for transistor-level simulation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 881-895	2.5	2
29	Efficient Thermal via Planning Approach and Its Application in 3-D Floorplanning. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 645-658	2.5	24
28	Noninvasive Study of the Human Heart using Independent Component Analysis **2006**,		1

27	Layer Minimization of Escape Routing in Area Array Packaging. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2006**,		2
26	Corner block list representation and its application to floorplan optimization. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2004**, 51, 228-233		22
25	Fast postplacement optimization using functional symmetries. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2004**, 23, 102-118	2.5	10
24	UTACO: a unified timing and congestion optimization algorithm for standard cell global routing. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2004**, 23, 358-365	2.5	5
23	Area minimization of power distribution network using efficient nonlinear programming techniques. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2004**, 23, 1086-1094	2.5	32
22	Reduced Order Modeling for RLC Interconnect Tree Using Hurwitz Polynomial. *Analog Integrated Circuits and Signal Processing*, **2002**, 31, 193-208	1.2	1
21	Empirical Study of Block Placement by Cluster Refinement. *VLSI Design*, **1999**, 10, 71-86		
20	Timing optimization for multisource nets: characterization and optimal repeater insertion. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **1999**, 18, 322-331	2.5	12
19	Routability improvement using dynamic interconnect architecture. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **1998**, 6, 498-501	2.6	2
18	Data flow partitioning with clock period and latency constraints. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **1997**, 44, 210-220		1
17	TIGER: an efficient timing-driven global router for gate array and standard cell layout design. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **1997**, 16, 1323-1331	2.5	16
16	A global router with a theoretical bound on the optimal solution. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **1996**, 15, 208-216	2.5	40
15	A wire length estimation technique utilizing neighborhood density equations. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **1996**, 15, 912-922	2.5	15
14	EARLY FEASIBILITY AND COST ASSESSMENT FOR MULTICHIP MODULE TECHNOLOGIES. *Selected Topics in Electornics and Systems*, **1996**, 25-42	0	
13	EARLY FEASIBILITY AND COST ASSESSMENT FOR MULTICHIP MODULE TECHNOLOGIES. *International Journal of High Speed Electronics and Systems*, **1995**, 06, 441-458	0.5	0
12	Design and implementation of a global router based on a new layout-driven timing model with three poles		2
11	Physical synthesis of energy-efficient networks-on-chip through topology exploration and wire style optimization		8
10	A mulitple level network approach for clock skew minimization with process variations		8

List of Publications

9	Arbitrary convex and concave rectilinear block packing based on corner block list	1
8	A buffer planning algorithm based on dead space redistribution	1
7	Floorplanning with consideration of white space resource distribution for repeater planning	1
6	Corner block list: an effective and efficient topological representation of non-slicing floorplan	30
5	RLC interconnect delay estimation via moments of amplitude and phase response	2
4	Finite state machine decomposition for I/O minimization	1
3	Optimal and efficient buffer insertion and wire sizing	20
2	New spectral linear placement and clustering approach	4
1	Skew Sensitivity Minimization Of Buffered Clock Tree	3