Michiko Inoue

List of Publications by Year
in descending order

73	484	1307594 7	1125743 13
papers	citations	h-index	g-index

78	78	78	242
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Eventually consistent distributed ledger despite degraded atomic broadcast. Concurrency Computation Practice and Experience, 2023, 35, e6199.	2.2	0
2	Unsupervised recycled FPGA detection using exhaustive nearest neighbor residual analysis. Japanese Journal of Applied Physics, 2022, 61, SC1076.	1.5	0
3	Systematic Unsupervised Recycled Field-Programmable Gate Array Detection. IEEE Transactions on Device and Materials Reliability, 2022, 22, 154-163.	2.0	1
4	Weakly Byzantine Gathering with a Strong Team. IEICE Transactions on Information and Systems, 2022, E105.D, 541-555.	0.7	2
5	Accurate Recycled FPGA Detection Using an Exhaustive-Fingerprinting Technique Assisted by WID Process Variation Modeling. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1626-1639.	2.7	7
6	Hardwareâ€“Software Co-Design for Decimal Multiplication. Computers, 2021, 10, 17.	3.3	2
7	Unsupervised Recycled FPGA Detection Based on Direct Density Ratio Estimation. , 2021, , .		4
8	Uniform bipartition in the population protocol model with arbitrary graphs. Theoretical Computer Science, 2021, , .	0.9	0
9	Gathering with a strong team in weakly Byzantine environments. , 2021, , .		3
10	Wafer-level Variation Modeling for Multi-site RF IC Testing via Hierarchical Gaussian Process. , 2021, , .		5
11	Study on High-Accuracy and Low-Cost Recycled FPGA Detection. , 2021, , .		0
12	Robust Fault-Tolerant Design Based on Checksum and On-Line Testing for Memristor Neural Network. , 2021, , .		0
13	Highly Reliable Memory Architecture Using Adaptive Combination of Proactive Aging-Aware In-Field Self-Repair and ECC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1688-1698.	2.7	5
14	Area-Efficient and Reliable Error Correcting Code Circuit Based on Hybrid CMOS/Memristor Circuit. Journal of Electronic Testing: Theory and Applications (JETTA), 2020, 36, 537-546.	1.2	1
15	Byzantine-Tolerant Gathering of Mobile Agents in Asynchronous Arbitrary Networks with Authenticated Whiteboards. IEICE Transactions on Information and Systems, 2020, E103.D, 1672-1682.	0.7	2
16	Eventually Consistent Distributed Ledger Relying on Degraded Atomic Broadcast. , 2019, , .		1
17	Low Cost Recycled FPGA Detection Using Virtual Probe Technique. , 2019, , .		8
18	Space-Optimal Population Protocols for Uniform Bipartition Under Global Fairness. IEICE Transactions on Information and Systems, 2019, E102.D, 454-463.	0.7	1

#	Article	IF	Citations
19	Test Coverage. , 2019, , 439-473.		1
20	Gathering of Mobile Agents in Asynchronous Byzantine Environments with Authenticated Whiteboards. Lecture Notes in Computer Science, 2019, , 85-99.	1.3	2
21	Variation-Aware Hardware Trojan Detection through Power Side-channel. , 2018, , .		18
22	Decimal Multiplication Using Combination of Software and Hardware. , 2018, , .		2
23	Artificial Neural Network Based Test Escape Screening Using Generative Model. , 2018, , .		11
24	Area-Efficient and Reliable Hybrid CMOS/Memristor ECC Circuit for ReRAM Storage. , 2018, , .		3
25	A Population Protocol for Uniform k-Partition Under Global Fairness. , 2018, , .		0
26	Byzantine-Tolerant Gathering of Mobile Agents in Arbitrary Networks with Authenticated Whiteboards. IEICE Transactions on Information and Systems, 2018, E101.D, 602-610.	0.7	7
27	An integrated DFT solution for power reduction in scan test applications by low power gating scan cell. The Integration VLSI Journal, 2017, 57, 108-124.	2.1	4
28	Detecting hardware Trojans without a Golden IC through clock-tree defined circuit partitions. , 2017, , .		13
29	Intra-Die-Variation-Aware Side Channel Analysis for Hardware Trojan Detection. , 2017, , .		5
30	An Effective and Sensitive Scan Segmentation Technique for Detecting Hardware Trojan. IEICE Transactions on Information and Systems, 2017, E100.D, 130-139.	0.7	9
31	An Efficient Silent Self-stabilizing 1-Maximal Matching Algorithm Under Distributed Daemon for Arbitrary Networks. Lecture Notes in Computer Science, 2017, , 93-108.	1.3	5
32	Byzantine Gathering in Networks with Authenticated Whiteboards. Lecture Notes in Computer Science, 2017, , 106-118.	1.3	3
33	Reliability enhancement of embedded memory with combination of aging-aware adaptive in-field self-repair and ECC. , 2016, , .		2
34	Reliability-Enhanced ECC-Based Memory Architecture Using In-Field Self-Repair. IEICE Transactions on Information and Systems, 2016, E99.D, 2591-2599.	0.7	1
35	An Efficient Silent Self-stabilizing 1-Maximal Matching Algorithm Under Distributed Daemon Without Global Identifiers. Lecture Notes in Computer Science, 2016, , 195-212.	1.3	6
36	An Efficient Silent Self-Stabilizing 1-Maximal Matching Algorithm in Anonymous Networks. Journal of Graph Algorithms and Applications, 2016, 20, 59-78.	0.4	5

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37	An effective scan segmentation approach to detect hardware Trojan in integrated circuits. , 2015, , .		0
38	An ECC-based memory architecture with online self-repair capabilities for reliability enhancement. , 2015, , .		6
39	Parallel Path Delay Fault Simulation for Multi/Many-Core Processors with SIMD Units. , 2014, , .		4
40	Memory block based scan-BIST architecture for application-dependent FPGA testing. , 2014, , .		1
41	A Scan-Based On-Line Aging Monitoring Scheme. Journal of Semiconductor Technology and Science, 2014, 14, 124-130.	0.4	9
42	Test Pattern Ordering and Selection for High Quality Test Set under Constraints. IEICE Transactions on Information and Systems, 2012, E95.D, 3001-3009.	0.7	3
43	A fast and accurate per-cell dynamic IR-drop estimation method for at-speed scan test pattern validation. , 2012, , .		19
44	A Failure Prediction Strategy for Transistor Aging. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1951-1959.	3.1	22
45	DART: Dependable VLSI test architecture and its implementation. , 2012, , .		24
46	Temperature-Variation-Aware Test Pattern Optimization. , 2011, , .		12
47	Faster-than-at-speed test for increased test quality and in-field reliability. , 2011, , .		24
48	Balanced Secure Scan: Partial Scan Approach for Secret Information Protection. Journal of Electronic Testing: Theory and Applications (JETTA), 2011, 27, 99-108.	1.2	4
49	Bipartite Full Scan Design: A DFT Method for Asynchronous Circuits. , 2010, , .		2
50	A method of unsensitizable path identification using high level design information. , 2010, , .		4
51	Capture in Turn Scan for Reduction of Test Data Volume, Test Application Time and Test Power. , 2010, , .		4
52	Seed Ordering and Selection for High Quality Delay Test. , 2010, , .		3
53	Aging test strategy and adaptive test scheduling for SoC failure prediction. , 2010, , .		3
54	Test pattern selection to optimize delay test quality with a limited size of test set. , 2010, , .		2

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55	Thermal-uniformity-aware X-filling to reduce temperature-induced delay variation for accurate at-speed testing. , 2010, , .		15
56	A response compactor for extended compatibility scan tree construction. , 2009, , .		4
57	A circuit failure prediction mechanism (DART) for high field reliability. , 2009, , .		27
58	Partial Scan Approach for Secret Information Protection. , 2009, , .		31
59	Hierarchical BIST: Test-per-clock BIST with low overhead. Electronics and Communications in Japan, 2007, 90, 47-58.	0.2	5
60	Design for Testability of Software-Based Self-Test for Processors. Proceedings of the Asian Test Symposium, 2006, , .	0.0	17
61	Instruction-Based Self-Testing of Delay Faults in Pipelined Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 1203-1215.	3.1	35
62	Non-scan Design for Single-Port-Change Delay Fault Testability. IPSJ Digital Courier, 2006, 2, 338-347.	0.3	0
63	Clustering algorithms in ad hoc networks. Electronics and Communications in Japan, 2005, 88, 51-59.	0.2	10
64	A layout adjustment problem for disjoint rectangles preserving orthogonal order. Systems and Computers in Japan, 2002, 33, 31-42.	0.2	7
65	Parallel algorithms for selection on the BSP and BSP* models. Systems and Computers in Japan, 2002, 33, 97-107.	0.2	2
66	Sequential Circuits with Combinational Test Generation Complexity under Single-Fault Assumption. Journal of Electronic Testing: Theory and Applications (JETTA), 2002, 18, 55-62.	1.2	2
67	A causal broadcast protocol for distributed mobile systems. Systems and Computers in Japan, 2001, 32, 65-75.	0.2	1
68	Parallelizability of some P-complete problems. Lecture Notes in Computer Science, 2000, , 116-122.	1.3	3
69	A cost optimal parallel algorithm for weighted distance transforms. Parallel Computing, 1999, 25, 405-416.	2.1	5
70	An approach to test synthesis from higher level. The Integration VLSI Journal, 1998, 26, 101-116.	2.1	1
71	Optimal wait-free clock synchronization protocol on a shared-memory multi-processor system. Lecture Notes in Computer Science, 1997, , 290-304.	1.3	1
72	Non-scan design for testable data paths using thru operation. Systems and Computers in Japan, 1997, 28, 60-68.	0.2	5

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73	Linear-time snapshot using multi-writer multi-reader registers. Lecture Notes in Computer Science, 1994, , 130-140.	1.3	22