Jeffrey Goeders

List of Publications by Year
in descending order

15	123	1937685 4	2053705 5
papers	citations	h-index	g-index

15	15	15	64
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Signal-Tracing Techniques for In-System FPGA Debugging of High-Level Synthesis Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 83-96.	2.7	38
2	Microcontroller Compiler-Assisted Software Fault Tolerance. IEEE Transactions on Nuclear Science, 2019, 66, 223-232.	2.0	28
3	Applying Compiler-Automated Software Fault Tolerance to Multiple Processor Platforms. IEEE Transactions on Nuclear Science, 2020, 67, 321-327.	2.0	14
4	Accelerating in-system FPGA debug of high-level synthesis circuits using incremental compilation techniques. , 2017, , .		8
5	Investigating How Software Characteristics Impact the Effectiveness of Automated Software Fault Tolerance. IEEE Transactions on Nuclear Science, 2021, 68, 1014-1022.	2.0	7
6	Architecture Exploration for HLS-Oriented FPGA Debug Overlays. , 2018, , .		6
7	An FPGA Overlay Architecture Supporting Rapid Implementation of Functional Changes during On-Chip Debug. , 2018, , .		5
8	An Overlay for Rapid FPGA Debug of Machine Learning Applications. , 2019, , .		5
9	Using Novel Configuration Techniques for Accelerated FPGA Aging. , 2020, , .		5
10	Approaches for FPGA Design Assurance. ACM Transactions on Reconfigurable Technology and Systems, 2022, 15, 1-29.	2.5	3
11	Unified On-Chip Software and Hardware Debug for HLS-Accelerated Programs. , 2018, , .		2
12	Using Physical and Functional Comparisons to Assure 3rd-Party IP for Modern FPGAs. , 2018, , .		1
13	Synchronizing On-Chip Software and Hardware Traces for HLS-Accelerated Programs. , 2019, , .		1
14	Enabling Long Debug Traces of HLS Circuits Using Bandwidth-Limited Off-Chip Storage Devices. , 2017, , .		0
15	Automated Software Compiler Techniques to Provide Fault Tolerance for Real-Time Operating Systems. , 2021, , .		0