Cheng-Ru Ho

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/7069687/publications.pdf

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8	118	1684188 5	2053705 5
papers	citations	h-index	g-index

8	8	8	154
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A Fractional-N Digital MDLL With Background Two-Point DTC Calibration. IEEE Journal of Solid-State Circuits, 2022, 57, 80-89.	5.4	7
2	Smoothing the Way for Digital Phase-Locked Loops: Clock Generation in the Future with Digital Signal Processing for Mitigating Spur and Interference. IEEE Microwave Magazine, 2019, 20, 80-97.	0.8	10
3	A fractional-N digital PLL with background-dither-noise-cancellation loop achieving <-62.5dBc worst-case near-carrier fractional spurs in 65nm CMOS. , 2018, , .		12
4	A Flash-Based Non-Uniform Sampling ADC With Hybrid Quantization Enabling Digital Anti-Aliasing Filter. IEEE Journal of Solid-State Circuits, 2017, 52, 2335-2349.	5.4	41
5	A Digital PLL With Feedforward Multi-Tone Spur Cancellation Scheme Achieving <â€“73 dBc Fractional Spur and <â€“110 dBc Reference Spur in 65 nm CMOS. IEEE Journal of Solid-State Circuits, 2016, 51, 3216-3230.	5.4	19
6	A Fractional-N DPLL With Calibration-Free Multi-Phase Injection-Locked TDC and Adaptive Single-Tone Spur Cancellation Scheme. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1111-1122.	5.4	16
7	Interference-induced DCO spur mitigation for digital phase locked loop in 65-nm CMOS. , 2016, , .		5
8	A fractional-N DPLL with adaptive spur cancellation and calibration-free injection-locked TDC in 65nm CMOS. , 2014, , .		8