# Tsutomu Yoshimura

List of Publications by Year
in descending order



| 16 | 105 | 1937685 4 | 1872680 6 |
|---|---|---|---|
| papers | citations | h-index | g-index |

| 16 | 16 | 16 | 88 |
|---|---|---|---|
| all docs | docs citations | times ranked | citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | Reexamination of SRAM Cell Write Margin Definitions in View of Predicting the Distribution. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 230-234. | 3.0 | 43 |
| 2 | Energy Efficient Stepwise Charging of a Capacitor Using a DC-DC Converter With Consecutive Changes of its Duty Ratio. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2194-2203. | 5.4 | 20 |
| 3 | Digital Mismatch Correction for Bandpass Sampling Four-Channel Time-Interleaved ADCs in Direct-RF Sampling Receivers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2007-2016. | 5.4 | 14 |
| 4 | Simultaneous enlargement of SRAM read/write noise margin by controlling virtual ground lines. , 2010, , . | | 5 |
| 5 | Analysis and modeling of response of external noise in oscillators. Analog Integrated Circuits and Signal Processing, 2016, 87, 313-325. | 1.4 | 4 |
| 6 | A Polyphase Decimation Filter for Time-Interleaved ADCs in Direct-RF Sampling Receivers. , 2018, , . | | 4 |
| 7 | Study of Injection Pulling of Oscillators in Phase-Locked Loops. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 321-332. | 3.1 | 4 |
| 8 | Accelerated evaluation method for the SRAM cell write margin using word line voltage shift. , 2011, , . | | 2 |
| 9 | A study of optimization for efficiency and power control in an electromagnetic WPT system. , 2013, , . | | 2 |
| 10 | Subharmonically injection-locked PLL with variable pulse-width injections. , 2015, , . | | 2 |
| 11 | Self-Coupling and Mutual Pulling in Phase-Locked Loops. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 3260-3271. | 5.4 | 2 |
| 12 | A 2.6GHz subharmonically injection-locked PLL with low-spur and wide-lock-range injection. , 2016, , . | | 1 |
| 13 | Study of mutual injection pulling in a 5-GHz, 0.18-Î¼m CMOS cascaded PLL. , 2018, , . | | 1 |
| 14 | Mitigation of Mutual Pulling in Two Phase-locked Loops. , 2021, , . | | 1 |
| 15 | Modeling and analysis of interference between phase-locked loops. , 2012, , . | | 0 |
| 16 | A Design of Engineering PBL on Embedded System for Novice Freshmen Students. , 2018, , . | | 0 |