Deepti Gola

List of Publications by Year
in descending order

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18	294	1040056 9	1199594 12
papers	citations	h-index	g-index

18	18	18	165
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Analytical Modeling of Channel Potential and Threshold Voltage of Double-Gate Junctionless FETs With a Vertical Gaussian-Like Doping Profile. IEEE Transactions on Electron Devices, 2016, 63, 2299-2305.	3.0	67
2	Dielectric pocket double gate junctionless FET: a new MOS structure with improved subthreshold characteristics for low power VLSI applications. Journal of Computational Electronics, 2016, 15, 502-507.	2.5	39
3	2-D Analytical Threshold Voltage Model for Dielectric Pocket Double-Gate Junctionless FETs by Considering Source/Drain Depletion Effect. IEEE Transactions on Electron Devices, 2017, 64, 901-908.	3.0	36
4	Subthreshold Modeling of Tri-Gate Junctionless Transistors With Variable Channel Edges and Substrate Bias Effects. IEEE Transactions on Electron Devices, 2018, 65, 1663-1671.	3.0	29
5	A Threshold Voltage Model of Tri-Gate Junctionless Field-Effect Transistors Including Substrate Bias Effects. IEEE Transactions on Electron Devices, 2017, 64, 3534-3540.	3.0	24
6	Analytical modeling of subthreshold characteristics of ion-implanted symmetric double gate junctionless field effect transistors. Materials Science in Semiconductor Processing, 2017, 58, 82-88.	4.0	22
7	Ferro-electric stacked gate oxide heterojunction electro-statically doped source/drain double-gate tunnel field effect transistors: A superior structure. Materials Science in Semiconductor Processing, 2017, 71, 161-165.	4.0	20
8	Static and Quasi-Static Drain Current Modeling of Tri-Gate Junctionless Transistor With Substrate Bias-Induced Effects. IEEE Transactions on Electron Devices, 2019, 66, 2876-2883.	3.0	17
9	Subthreshold Characteristic Analysis and Models for Tri-Gate SOI MOSFETs Using Substrate Bias Induced Effects. IEEE Nanotechnology Magazine, 2019, 18, 329-335.	2.0	15
10	Subthreshold Modeling of Graded Channel Double Gate Junctionless FETs. Silicon, 2021, 13, 1231-1238.	3.3	8
11	Thermal Noise Models for Trigate Junctionless Transistors Including Substrate Bias Effects. IEEE Transactions on Electron Devices, 2020, 67, 263-269.	3.0	6
12	Temperature Sensitivity Analysis of Double Gate Junctionless Field Effect Transistor with Vertical Gaussian Doping Profile. , 2016, , .		4
13	An analytical subthreshold current model of short-channel symmetrical double gate-all-around (DGAA) field-effect-transistors. , 2017, , .		3
14	Performance evaluation of double gate junctionless field effect transistor with vertical Gaussian doping profile. , 2016, , .		1
15	Analytical Modeling of Analog/RF Parameters for Trigate Junctionless Field Effect Transistor Incorporating Substrate Biasing Effects. , 2019, , .		1
16	Subthreshold Performance Analysis of Double-Fin Multi-channel Junctionless Transistor with Substrate Bias Effects. , 2019, , .		1
17	Self-heating and Negative Differential Conductance Improvement by Substrate Bias Voltage in Tri-gate Junctionless Transistor. Silicon, 2022, 14, 2219-2224.	3.3	1
18	Investigation of Thermal Noise in Trigate Junctionless Transistor. , 2019, , .		0