Bo-Cheng Lai

List of Publications by Year
in descending order

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42 papers	169 citations	1478505 6 h-index	1474206 9 g-index
42 all docs	42 docs citations	42 times ranked	128 citing authors

#	Article	IF	Citations
1	DSIM: Distributed Sequence Matching on Near-DRAM Accelerator for Genome Assembly. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2022, 12, 486-499.	3.6	4
2	Distributed Sorting Architecture on Multiple FPGA. , 2022, , .		0
3	DASC: A DRAM Data Mapping Methodology for Sparse Convolutional Neural Networks. , 2022, , .		0
4	Air Pollution Is Associated with Poor Cognitive Function in Taiwanese Adults. International Journal of Environmental Research and Public Health, 2021, 18, 316.	2.6	13
5	Parametric Study of Performance of Remote Photopletysmography System. , 2021, , .		1
6	The Impact of the Synergistic Effect of Temperature and Air Pollutants on Chronic Lung Diseases in Subtropical Taiwan. Journal of Personalized Medicine, 2021, 11, 819.	2.5	8
7	On Reconfiguring Memory-Centric AI Edge Devices for CIM. , 2021, , .		2
8	Selective bypassing and mapping for heterogeneous applications on GPGPUs. Journal of Parallel and Distributed Computing, 2020, 142, 106-118.	4.1	0
9	Air Pollutants Interaction and Gender Difference on Bone Mineral Density T-Score in Taiwanese Adults. International Journal of Environmental Research and Public Health, 2020, 17, 9165.	2.6	17
10	A Two-Directional BigData Sorting Architecture on FPGAs. IEEE Computer Architecture Letters, 2020, 19, 72-75.	1.5	4
11	REMAP+: An Efficient Banking Architecture for Multiple Writes of Algorithmic Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 660-671.	3.1	2
12	Dataflow and microarchitecture coâ€optimisation for sparse CNN on distributed processing element accelerator. IET Circuits, Devices and Systems, 2020, 14, 1185-1194.	1.4	1
13	Efficient Write Scheme for Algorithm-Based Multi-Ported Memory. , 2019, , .		3
14	Enhancing Utilization of SIMD-Like Accelerator for Sparse Convolutional Neural Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1218-1222.	3.1	9
15	Supporting compressed-sparse activations and weights on SIMD-like accelerator for sparse convolutional neural networks. , 2018, , .		9
16	Towards high performance data analytic on heterogeneous many-core systems: A study on Bayesian Sequential Partitioning. Journal of Parallel and Distributed Computing, 2018, 122, 36-50.	4.1	1
17	Efficient Designs of Multiported Memory on FPGA. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 139-150.	3.1	18
18	A software technique to enhance register utilization of Convolutional Neural Networks on GPGPUs. , 2017, , .		1

#	Article	IF	Citations
19	An Efficient Hierarchical Banking Structure for Algorithmic Multiported Memory on FPGA. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2776-2788.	3.1	5
20	Scalable mutli-layer barrier synchronization on NoC. , 2016, , .		1
21	A Quantitative Method to Data Reuse Patterns of SIMT Applications. IEEE Computer Architecture Letters, 2016, 15, 73-76.	1.5	0
22	Computation and Communication Aware task graph Scheduling on multi-GPU systems. , 2015, , .		0
23	BRAM efficient multi-ported memory on FPGA. , 2015, , .		7
24	Design of Application Specific Throughput Processor for Matrix Operations. , 2015, , .		1
25	Self adaptable multithreaded object detection on embedded multicore systems. Journal of Parallel and Distributed Computing, 2015, 78, 25-38.	4.1	4
26	A High-Performance Double-Layer Counting Bloom Filter for Multicore Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2473-2486.	3.1	3
27	A Cache Hierarchy Aware Thread Mapping Methodology for GPGPUs. IEEE Transactions on Computers, 2015, 64, 884-898.	3.4	9
28	Power-Efficient Instancy Aware DRAM Scheduling. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2015, E98.A, 942-953.	0.3	0
29	A distributed thread scheduler for dynamic multithreading on throughput processors. , 2013, , .		0
30	Cache Capacity Aware Thread Scheduling for Irregular Memory Access on many-core GPGPUs. , 2013, , .		6
31	A Locality-Aware Dynamic Thread Scheduler for GPGPUs. , 2013, , .		0
32	Memory capacity aware non-blocking data transfer on GPGPU. , 2013, , .		3
33	A highly parallel design of image surface layout recovering on GPGPU. , 2012, , .		0
34	Reduce Data Coherence Cost with an Area Efficient Double Layer Counting Bloom Filter. , 2012, , .		3
35	Thread affinity mapping for irregular data access on shared Cache GPGPU. , 2012, , .		6
36	Multi-level parallelism analysis of face detection on a shared memory multi-core system. , 2011, , .		8

#	Article	IF	Citations
37	Classifier Grouping to Enhance Data Locality for a Multi-threaded Object Detection Algorithm. , 2011, , .		4
38	FDPrior: A force-directed based parallel partitioning algorithm for three dimensional integrated circuits on GPGPU. , 2011, , .		2
39	Data locality optimization for a parallel object detection on embedded multi-core systems. , 2011, , .		5
40	Fast parallel analysis of dynamic contrast-enhanced magnetic resonance imaging on GPGPU. , 2010, , .		0
41	Unleash the parallelism of 3DIC partitioning on GPGPU. , 2010, , .		2
42	A Cost-Effective Latency-Aware Memory Bus for Symmetric Multiprocessor Systems. IEEE Transactions on Computers, 2008, 57, 1714-1719.	3.4	7